

DA14531 Pro Development Kit

Design Name	d2632-db-qfn24_vF2
Ref. Number	376-04-F
Version	F1.2
Date	August 09, 2019
Designer	Kalliopi Liantinioti

Configuration note

NOTE box

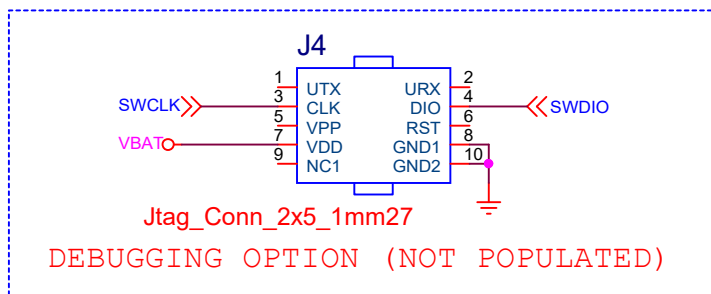
Changes in this Version.

History Table

Version	Date	Comments
A00	08 / Aug / 2018	Draft Release
	09 / Aug / 2018	Added option for hardware reset (P0_0 - R30) Added CIB debugging option (J4) Corrected mismatch in function notes (purple names) for MISO/SCLK
A1.0	17 / Aug / 2018	Released to manufacturing
		Added options for SWDIO (R31, R32) Default option for SWDIO set to P0_10 (R31) Version number set to C (matching the layout version)
C1.0	17 / Aug / 2018	Released to manufacturing
		Set default configuration: SPI bus and JTAG: • R1 to R12 changed to 36 Ohms instead of 100 ohms • Y2 (32.768KHz - NP) type changed to SC20S-7PF20PPM • R23 R24 R25 R26 R27 R28 R29 set as not populated
C1.1	30 / Nov / 2018	
		Set JTAG SWDIO on P0_5 (not on P0_10 as in datasheet) • R31 = No pop • R15 = 0 Added Matching circuit Z1, Z3 • Z3 = 4.6nH / LQW15AN4N6B80D • Z1 = 1pF
C1.2	10 / Jan / 2019	
		BOM modifications for DCDC power optimization: • Changed L1 from BRL1608T2R2M to CBMF1608T2R2M • Changed C1, C2 from 10uF to 2.2uF Set JTAG SWDIO on P0_10 (as in datasheet) • R31 = 0 • R15 = No Pop
C1.3	01 / Feb / 2019	
D1.0	04 / Feb / 2019	Changed L1 from CBMF1608T2R2M to DFE201610E-2R2M
E1.0	15 / May / 2019	Changed C2 to 4.7uF Added NP resistor R33 Layout modification: Removed restangle on top legend around U1
F1.0	03/ July / 2019	Added placeholder for pi-shaped CLC filter (Z1, Z2, Z3) Changed RF matching components to : Z4, Z5 , Z6 Added placeholder for decoupling capacitors: C6, C7 Added resistors R34, R35
F1.1	10/ July / 2019	Changed C2 from 4.7uF to 10uF
F1.2	09 / Aug / 2019	Changed R11 to N.P.

TP11 FIDUCIAL

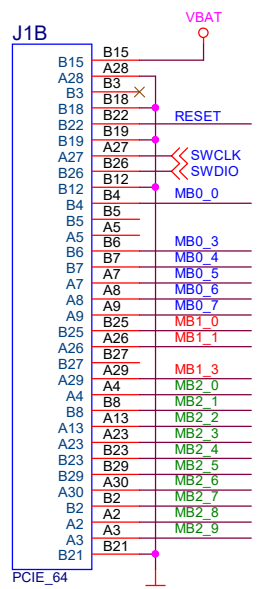
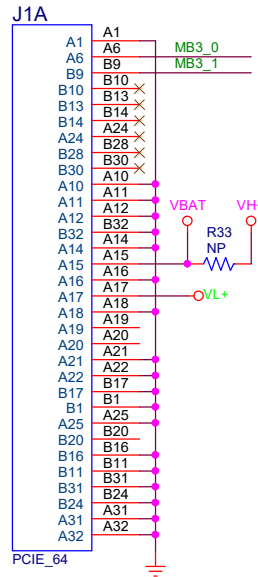
TP12 FIDUCIAL



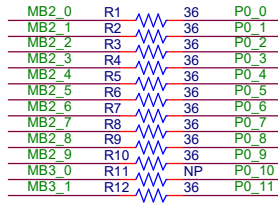
<Variant Name>

		Dialog Semiconductor N.E.O. Athinon- Patron 15 26441, Patra, Greece tel. (+30) 2610390940 fax. (+30) 2610390941
Title : DA14531/D2632 Development Kit Daughterboard		
Doc. Nr. 376-04-F	Designer: Kalliopi Liantinioti	Rev:F
Date: Monday, August 12, 2019	Sheet: 1 of 2	

Card Edge Connector (PCI-E)



BREAKOUT HEADERS



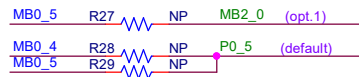
JTAG



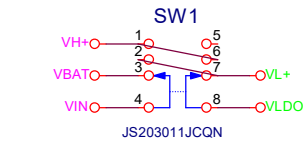
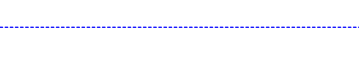
SPI FLASH



4-PIN UART



1-WIRE UART(2)



POWER MODE SELECTION

APPLICABLE ONLY TO DA14580DEVKT-P_B/C

FOR DA145xxDEVKT-P_D SET TO BUCK (H) AND SELECT THE DESIRED MODE FROM THE MB

