Abstract

This application note provides information on powering the Xilinx Spartan-7 family of devices.
Power Solutions for Xilinx® Spartan®-7 Devices

Contents
Abstract ........................................................................................................................................... 1
Contents ........................................................................................................................................... 2
Figures ............................................................................................................................................... 2
Tables ............................................................................................................................................... 3

■ Terms and Definitions .................................................................................................................. 4
■ References ....................................................................................................................................... 4
■ Introduction .................................................................................................................................... 5
■ Getting Started ............................................................................................................................... 5
  □ The Spartan-7 ............................................................................................................................... 5
  □ The Dialog DA9062 ...................................................................................................................... 6
  The DA9062 Regulators .................................................................................................................. 7
  The DA9062 PCB Footprint .......................................................................................................... 7
  Typical Bill of Materials .............................................................................................................. 8
  □ Mapping to the DA9062 .............................................................................................................. 9
    Flexibility9
    DA9062 Additional Features ..................................................................................................... 9
    Working with the DA9062 .......................................................................................................... 10
  □ Bench Measurements .................................................................................................................. 12
    Power-On Sequence ................................................................................................................... 12
    Buck Efficiency ......................................................................................................................... 13
    Static Load Regulation ............................................................................................................. 14
    Buck Transient Load Regulation ............................................................................................... 16
    Reference Measurements .......................................................................................................... 21
■ Conclusions .................................................................................................................................. 22
Revision History ............................................................................................................................. 23

Figures
Figure 1: The Spartan-7 Power Rail Requirements ........................................................................... 5
Figure 2: DA9062 Block Diagram .................................................................................................... 6
Figure 3: DA9062 Solution Footprint ............................................................................................... 7
Figure 4: The DA9062 Evaluation Board .......................................................................................... 10
Figure 5: The DA9062 SmartCanvas GUI ....................................................................................... 11
Figure 6: The SmartCanvas Drag and Drop Sequence Tool ............................................................ 11
Figure 7: Spartan-7 Power-On Sequence .......................................................................................... 12
Figure 8: Buck1 Efficiency with \( V_{\text{OUT}} = 0.95 \text{ V} \) and \( V_{\text{IN}} = 5 \text{ V} \) and 3.6 \( V \) .................................... 13
Figure 9: Buck2 Efficiency with \( V_{\text{OUT}} = 1.35 \text{ V} \) and \( V_{\text{IN}} = 5 \text{ V} \) and 3.6 \( V \) .................................... 13
Figure 10: Buck3 Efficiency with \( V_{\text{OUT}} = 1.8 \text{ V} \) and \( V_{\text{IN}} = 5 \text{ V} \) and 3.6 \( V \) .................................... 14
Figure 11: Buck1 Static Load Regulation ........................................................................................... 14
Figure 12: Buck2 Static Load Regulation ........................................................................................... 15
Figure 13: Buck3 Static Load Regulation ........................................................................................... 15
Figure 14: LDO2 Static Load Regulation ........................................................................................... 16
Figure 15: VCCINT (Buck1) Transient Response, 310 mA to 990 mA step ........................................ 17
Figure 16: VCCINT (Buck1) Transient Response, 1 A Step ............................................................... 17
Figure 17: VDDQ (Buck2) Transient Response, \( V_{\text{OUT}} = 1.35 \text{ V} \), 1 A Step ................................... 18
Figure 18: VDDQ (Buck2) Transient Response, \( V_{\text{OUT}} = 1.5 \text{ V} \), 1 A Step ..................................... 18
Figure 19: VCCIO (Buck3) Transient Response, \( V_{\text{OUT}} = 2.5 \text{ V} \), 1 A Step ..................................... 19
Power Solutions for Xilinx® Spartan®-7 Devices

Figure 20: VCCIO (Buck3) Transient Response, $V_{\text{OUT}} = 2.5$ V, 1.25 A Step ............................................. 19
Figure 21: VCCIO (Buck3) Transient Response, $V_{\text{OUT}} = 3.3$ V, 1 A Step ............................................. 20
Figure 22: VCCIO (Buck3) Transient Response, $V_{\text{OUT}} = 3.3$ V, 1.25 A Step ............................................. 20
Figure 23: $V_{\text{REF}}$ Over Temperature ................................................................. 21
Figure 24: $I_{\text{REF}}$ Over Temperature ................................................................. 21
Figure 25: VDDCORE Over Temperature .............................................................. 22

Tables

Table 1: Spartan-7 Power Rail Requirements ................................................................. 5
Table 2: DA9062 Regulator Summary ........................................................................ 7
Table 3: DA9062 Bill of Materials .............................................................................. 8
Table 4: DA9062 Mapping for Spartan-7 ................................................................. 9
Table 5: VCCINT Transient Load Results ................................................................. 16
Table 6: VDDQ Transient Load Results .................................................................. 18
Table 7: VCCIO Transient Load Results .................................................................. 19
Power Solutions for Xilinx® Spartan®-7 Devices

■ Terms and Definitions

GUI  Graphical User Interface
PMIC  Power Management Integrated Circuit
DA906x  Dialog DA9061, DA9062, DA9063, and DA9063L
DVC  Dynamic Voltage Control
DVS  Dynamic Voltage Scaling, analogous to DVC
MPSoC  Multiprocessor System-on-Chip
OTP  One-Time Programmable (memory)
RTC  Real-Time Clock
SoC  System-on-Chip

■ References

[3]  DA9061, Datasheet, Dialog Semiconductor, Dialog Website Link
[4]  DA9062, Datasheet, Dialog Semiconductor, Dialog Website Link
[5]  DA9063, Datasheet, Dialog Semiconductor, Dialog Website Link
[6]  DA9063L, Datasheet, Dialog Semiconductor, Dialog Website Link
[8]  UM-PM-008, SmartCanvas™ DA9061/2 User Manual, Dialog Semiconductor, Dialog Website Link
[10]  Spartan-7 FPGAs Data Sheet: DC and AC Switching Characteristics, Xilinx, Link
Power Solutions for Xilinx® Spartan®-7 Devices

■ Introduction

The Xilinx Spartan-7 family of FPGA devices is part of the Xilinx All Programmable Cost-Optimized Portfolio. To fully realize the performance of a Spartan-7 device requires an optimized power management solution. The Dialog DA9062 PMIC provides flexibility to match the requirements of most FPGA designs while maximizing performance and integration, and minimizing the PCB footprint.

■ Getting Started

The following sections introduce the basic power rail requirements of the Spartan-7 devices along with the capabilities of the Dialog DA9062 PMIC, and show why they are the perfect partners.

□ The Spartan-7

Table 1: Spartan-7 Power Rail Requirements

<table>
<thead>
<tr>
<th>Rail</th>
<th>Voltage (V)</th>
<th>Load (A)</th>
</tr>
</thead>
<tbody>
<tr>
<td>VCCINT</td>
<td>0.95 or 1</td>
<td>0.3 to 2.5</td>
</tr>
<tr>
<td>VCCBRAM</td>
<td>0.95 or 1</td>
<td>0.1</td>
</tr>
<tr>
<td>VCCAUX</td>
<td>1.8</td>
<td>0.15 to 0.35</td>
</tr>
<tr>
<td>VCCADC</td>
<td>1.8</td>
<td></td>
</tr>
<tr>
<td>VREFP</td>
<td>1.25</td>
<td></td>
</tr>
<tr>
<td>VCCIO</td>
<td>1.2 to 3.3</td>
<td>0.2 to 2.5</td>
</tr>
<tr>
<td>VDDQ</td>
<td>1.35 to 1.5</td>
<td>2</td>
</tr>
<tr>
<td>VREFCA</td>
<td></td>
<td>0.01</td>
</tr>
<tr>
<td>VTT</td>
<td></td>
<td>1</td>
</tr>
</tbody>
</table>

Figure 1: The Spartan-7 Power Rail Requirements
The Dialog DA9062 flexible power management IC integrates four bucks and four LDOs capable of supplying individual rails of up to 2.5 A. This device ideally matches the requirements of the Spartan-7 family of devices.

Figure 2: DA9062 Block Diagram
The DA9062 Regulators

Table 2: DA9062 Regulator Summary

<table>
<thead>
<tr>
<th>Regulator</th>
<th>Supplied Voltage (V)</th>
<th>Supplied Max. Current (A)</th>
<th>External Component</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>Buck1</td>
<td>0.3 to 1.57</td>
<td>2.5</td>
<td>1.0 μH / 2 x 47 μF</td>
<td>3 MHz, DVS with variable slew rate, 10 mV steps</td>
</tr>
<tr>
<td>Buck2</td>
<td>0.3 to 1.57</td>
<td>2.5</td>
<td>1.0 μH / 2 x 47 μF</td>
<td>3 MHz, DVS with variable slew rate, 10 mV steps, can be combined with Buck1 as a 5 A dual-phase buck</td>
</tr>
<tr>
<td>Buck3</td>
<td>0.8 to 3.34</td>
<td>2.0</td>
<td>1.0 μH / 2 x 22 μF or 2 x 47 μF</td>
<td>3 MHz, DVS with variable slew rate, 20 mV steps</td>
</tr>
<tr>
<td>Buck4</td>
<td>0.53 to 1.8</td>
<td>1.5</td>
<td>1.0 μH / 2 x 22 μF or 2 x 47 μF</td>
<td>3 MHz, DVS with variable slew rate, 10 mV steps, can be used as a DDR VTT supply</td>
</tr>
<tr>
<td>LDO1</td>
<td>0.9 to 3.6</td>
<td>0.1</td>
<td>1.0 μF</td>
<td>Programmable in 50 mV steps, can be configured as an ‘always-on’ supply</td>
</tr>
<tr>
<td>LDO2</td>
<td>0.9 to 3.6</td>
<td>0.3</td>
<td>2.2 μF</td>
<td>Programmable in 50 mV steps</td>
</tr>
<tr>
<td>LDO3</td>
<td>0.9 to 3.6</td>
<td>0.3</td>
<td>2.2 μF</td>
<td>Programmable in 50 mV steps</td>
</tr>
<tr>
<td>LDO4</td>
<td>0.9 to 3.6</td>
<td>0.3</td>
<td>2.2 μF</td>
<td>Programmable in 50 mV steps</td>
</tr>
</tbody>
</table>

The DA9062 PCB Footprint

The high level of integration along with the 3 MHz switching frequency results in a compact footprint. Figure 3 is an example footprint including all of the required passive components. The total area is less than 420 mm². This is achieved with all of the components on the top side of the PCB and without the use of over-aggressive placement. This area could be further reduced by placing some of the capacitors on the reverse of the PCB and by more aggressive spacing rules. As shown, there is significant unused space in the calculated area, possibly up to 25 %. See the DA9062 Performance board data pack for more details [11].

Figure 3: DA9062 Solution Footprint
### Table 3: DA9062 Bill of Materials

<table>
<thead>
<tr>
<th>Qty</th>
<th>Description</th>
<th>Value</th>
<th>Tol.</th>
<th>Rating</th>
<th>Dielectric</th>
<th>Manufacturer</th>
<th>Manufacturer Part Number</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>DA9062 QFN40</td>
<td>DA9062</td>
<td></td>
<td></td>
<td></td>
<td>Dialog</td>
<td>DA9062</td>
</tr>
<tr>
<td>2</td>
<td>TFM252010 Series SMD Inductor</td>
<td>1 µH</td>
<td>±20%</td>
<td>Isat=3.5 A</td>
<td></td>
<td>TDK</td>
<td>TFM252010A-1R0M</td>
</tr>
<tr>
<td>2</td>
<td>TFM201610 Series SMD Inductor</td>
<td>1 µH</td>
<td>±20%</td>
<td>Isat=2.9 A</td>
<td></td>
<td>TDK</td>
<td>TFM201610A-1R0M</td>
</tr>
<tr>
<td>4</td>
<td>0402 (1005 Metric) SMD Resistor</td>
<td>100 kΩ</td>
<td>±1%</td>
<td>0.063 W</td>
<td></td>
<td>Yageo</td>
<td>RC0402FR-07100KL</td>
</tr>
<tr>
<td>1</td>
<td>0402 (1005 Metric) SMD Resistor</td>
<td>200 kΩ</td>
<td>±1%</td>
<td>0.063 W</td>
<td></td>
<td>Yageo</td>
<td>RC0402FR-07200KL</td>
</tr>
<tr>
<td>2</td>
<td>0402 (1005 Metric) SMD Capacitor</td>
<td>15 pF</td>
<td>±5%</td>
<td>50 V</td>
<td>COG/NPO</td>
<td>Murata</td>
<td>GRM1555C1H150J1Z01D</td>
</tr>
<tr>
<td>2</td>
<td>0402 (1005 Metric) SMD Capacitor</td>
<td>100 nF</td>
<td>±10%</td>
<td>10 V</td>
<td>X5R</td>
<td>Murata</td>
<td>GRM155R61A104KA01D</td>
</tr>
<tr>
<td>1</td>
<td>0402 (1005 Metric) SMD Capacitor</td>
<td>470 nF</td>
<td>±10%</td>
<td>10 V</td>
<td>X5R</td>
<td>Murata</td>
<td>GRM155R61A474KE15D</td>
</tr>
<tr>
<td>4</td>
<td>0402 (1005 Metric) SMD Capacitor</td>
<td>1 µF</td>
<td>±10%</td>
<td>10 V</td>
<td>X5R</td>
<td>Murata</td>
<td>GRM155R61A105KE15D</td>
</tr>
<tr>
<td>4</td>
<td>0805 (2012 Metric) SMD Capacitor</td>
<td>22 µF</td>
<td>±20%</td>
<td>10 V</td>
<td>X5R</td>
<td>Taiyo Yuden</td>
<td>LMK212BJ226MG-T</td>
</tr>
<tr>
<td>5</td>
<td>0402 (1005 Metric) SMD Capacitor</td>
<td>2.2 µF</td>
<td>±20%</td>
<td>6.3 V</td>
<td>X5R</td>
<td>Murata</td>
<td>GRM155R60J225ME95</td>
</tr>
<tr>
<td>8</td>
<td>0805 (2012 Metric) SMD Capacitor</td>
<td>47 µF</td>
<td>±20%</td>
<td>4 V</td>
<td>X5R</td>
<td>Murata</td>
<td>GRM219R60G476M</td>
</tr>
</tbody>
</table>

**NOTE**

The BoM does not include the 32 kHz crystal or the backup battery cell as these are optional components dependent on the application requirements.
Mapping to the DA9062

Comparing the Spartan-7 power rail requirements from Table 1 with the DA9062 available regulators in Table 2, it is clear to see that the DA9062 is a good match for designs using the Spartan-7.

Mapping the Spartan-7 on to the DA9062 rails is shown in Table 4.

Table 4: DA9062 Mapping for Spartan-7

<table>
<thead>
<tr>
<th>Spartan-7</th>
<th>DA9062</th>
</tr>
</thead>
<tbody>
<tr>
<td>Rail</td>
<td>Voltage (V)</td>
</tr>
<tr>
<td>VCCINT</td>
<td>0.95/1</td>
</tr>
<tr>
<td>VCCBRAM</td>
<td>0.95/1</td>
</tr>
<tr>
<td>VCCAUX</td>
<td>1.8</td>
</tr>
<tr>
<td>VCCADC</td>
<td>1.8</td>
</tr>
<tr>
<td>VREFP</td>
<td>1.25</td>
</tr>
<tr>
<td>VCCIO</td>
<td>1.2 to 3.3</td>
</tr>
<tr>
<td>VDDQ</td>
<td>1.35 to 1.5</td>
</tr>
<tr>
<td>VREFCA</td>
<td>0.01</td>
</tr>
<tr>
<td>VTT</td>
<td></td>
</tr>
</tbody>
</table>

Flexibility

The DA9062 has four LDO regulators, so there are three spare regulators that can be used to provide power to additional parts of the system, or to supply additional voltage IO domains.

The voltage required to supply the VCCINT rail is either 0.95 V or 1.0 V.

The voltage required to supply the VDDQ rail is either 1.35 V or 1.5 V.

The DA9062 can be configured to provide two different output voltages depending on the state of a GPIO. A single configuration of the DA9062 can therefore easily fulfil the requirements of many Spartan-7 designs.

For designs not using DDR memory, or not requiring DDR termination, Buck4 can be configured as a normal buck to provide an extra supply rail for IO or any other requirement of the system. In applications where the additional rail is not required, the Dialog DA9061 should be considered.

For more demanding designs, Dialog has a range of System and Sub PMICS that can be used to build a power tree that will meet your needs, see http://www.dialog-semiconductor.com/power-management for more information.

DA9062 Additional Features

Along with the buck and LDO regulators, the DA9062 also includes a range of additional features that are vital to most systems.

- Supply rail qualification: The DA9062 can monitor the incoming supply to prevent the system starting if a suitable supply is not available. A warning will be generated if the supply falls below a programmed level.
- Low power RTC with alarm function and 32 kHz output.
- System RESET control: The DA9062 provides a system RESET signal that is used to hold the system in RESET until all supply rails are available.
- System Watchdog: The watchdog can be used to reset the system in the case that the system becomes unresponsive.
Working with the DA9062

The DA9062 Evaluation kit includes a flexible evaluation board to allow access to all of the key features of the part. The evaluation kit also includes the Dialog SmartCanvas™ GUI which simplifies the control and configuration of the DA9062.

Figure 4: The DA9062 Evaluation Board
Figure 5: The DA9062 SmartCanvas GUI

Figure 6: The SmartCanvas Drag and Drop Sequence Tool
Bench Measurements

This section provides some basic performance measurements made using the DA9062 Evaluation kit.

The following measurements are included:

- power-on sequence
- buck efficiency
- static load regulation.
- buck transient load regulation
- reference measurements

Power-On Sequence

![Figure 7: Spartan-7 Power-On Sequence]
Buck Efficiency

**Figure 8: Buck1 Efficiency with** $V_{\text{OUT}} = 0.95$ V and $V_{\text{IN}} = 5$ V and 3.6 V

**Figure 9: Buck2 Efficiency with** $V_{\text{OUT}} = 1.35$ V and $V_{\text{IN}} = 5$ V and 3.6 V
Figure 10: Buck3 Efficiency with $V_{OUT} = 1.8$ V and $V_{IN} = 5$ V and 3.6 V

Static Load Regulation

The following static load regulation plots show the variation on the output voltage over a sweep of the load. The buck regulators were running in Auto mode. The change in slope at approximately 300 mA is where the buck transitions from PFM to PWM.

Figure 11: Buck1 Static Load Regulation
Figure 12: Buck2 Static Load Regulation

Figure 13: Buck3 Static Load Regulation
Buck Transient Load Regulation

For the transient measurements in this section, the oscilloscope is configured as follows:

- Channel 1 (Yellow) shows the regulator output. The output was AC coupled, The buck was set to 0.95 V. The Min and Max measurements show the maximum excursion during the transient event.
- Channel 2 (Blue) shows the transient load being applied. The Low and High measurements were configured to show the levels of the current pulse waveform. The pulse duration was set to 10 µs.
- Channel 3 (Magenta), where shown, displays the DC coupled output voltage.
- The “a” and “b” horizontal cursors show the Xilinx specification limits for the specific voltage rail.

In Table 5, Table 6, and Table 7, the results are given for the transient as a percentage of the maximum load for the regulator. For example, 625 mA is 25 % of 2.5 A. The ±3 % specification is then calculated in mV for comparison against the measured result.

Table 5: VCCINT Transient Load Results

<table>
<thead>
<tr>
<th>VCCINT (V)</th>
<th>Low (mA)</th>
<th>High (mA)</th>
<th>%</th>
<th>Spec. Limit (mV)</th>
<th>Measured (mV)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>-3%</td>
<td>-3%</td>
</tr>
<tr>
<td>0.95</td>
<td>310</td>
<td>990</td>
<td>25</td>
<td>-28.5</td>
<td>-28.5</td>
</tr>
<tr>
<td>0.95</td>
<td>310</td>
<td>1310</td>
<td>40</td>
<td>-28.5</td>
<td>-20.8</td>
</tr>
</tbody>
</table>

Figure 14: LDO2 Static Load Regulation
Figure 15: VCCINT (Buck1) Transient Response, 310 mA to 990 mA step

Figure 16: VCCINT (Buck1) Transient Response, 1 A Step
### Table 6: VDDQ Transient Load Results

<table>
<thead>
<tr>
<th>VDDQ (V)</th>
<th>Transient Load</th>
<th>Spec. Limit (mV)</th>
<th>Measured (mV)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Low (mA)</td>
<td>High (mA)</td>
<td>%</td>
</tr>
<tr>
<td>1.35</td>
<td>310</td>
<td>1310</td>
<td>40 %</td>
</tr>
<tr>
<td>1.5</td>
<td>310</td>
<td>1310</td>
<td>40 %</td>
</tr>
</tbody>
</table>

**Figure 17:** VDDQ (Buck2) Transient Response, $V_{OUT} = 1.35$ V, 1 A Step

**Figure 18:** VDDQ (Buck2) Transient Response, $V_{OUT} = 1.5$ V, 1 A Step
Table 7: VCCIO Transient Load Results

<table>
<thead>
<tr>
<th>VCCIO (V)</th>
<th>Transient Load</th>
<th>Spec. Limit (mV)</th>
<th>Measured (mV)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Low (mA)</td>
<td>High (mA)</td>
<td>-3%</td>
</tr>
<tr>
<td>2.5</td>
<td>310</td>
<td>1310</td>
<td>-75</td>
</tr>
<tr>
<td>2.5</td>
<td>310</td>
<td>1570</td>
<td>-75</td>
</tr>
<tr>
<td>3.3</td>
<td>310</td>
<td>1310</td>
<td>-99</td>
</tr>
<tr>
<td>3.3</td>
<td>310</td>
<td>1570</td>
<td>-99</td>
</tr>
</tbody>
</table>

Figure 19: VCCIO (Buck3) Transient Response, V_OUT = 2.5 V, 1 A Step

Figure 20: VCCIO (Buck3) Transient Response, V_OUT = 2.5 V, 1.25 A Step
Figure 21: VCCIO (Buck3) Transient Response, $V_{OUT} = 3.3\, \text{V}$, 1 A Step

Figure 22: VCCIO (Buck3) Transient Response, $V_{OUT} = 3.3\, \text{V}$, 1.25 A Step
Reference Measurements

The operating performance of the PMIC is affected by the performance of the voltage and current references. This section shows the performance of the voltage and current references over temperature.

Figure 23: $V_{\text{REF}}$ Over Temperature

Figure 24: $I_{\text{REF}}$ Over Temperature
Conclusions

By providing a high level of integration and high efficiency in a small PCB footprint, the Dialog DA9062 can be seen to be an ideal partner to the Xilinx Spartan-7 family of devices.
### Revision History

<table>
<thead>
<tr>
<th>Revision</th>
<th>Date</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.0</td>
<td>01-Jun-2017</td>
<td>Initial version.</td>
</tr>
<tr>
<td>1.1</td>
<td>31-Aug-2017</td>
<td>Added Section: Bench Measurement.</td>
</tr>
<tr>
<td>1.2</td>
<td>10-Jan-2018</td>
<td>Corrected application note number.</td>
</tr>
</tbody>
</table>
Power Solutions for Xilinx® Spartan®-7 Devices

Status Definitions

<table>
<thead>
<tr>
<th>Status</th>
<th>Definition</th>
</tr>
</thead>
<tbody>
<tr>
<td>DRAFT</td>
<td>The content of this document is under review and subject to formal approval, which may result in modifications or additions.</td>
</tr>
<tr>
<td>APPROVED or unmarked</td>
<td>The content of this document has been approved for publication.</td>
</tr>
</tbody>
</table>

Disclaimer

Information in this document is believed to be accurate and reliable. However, Dialog Semiconductor does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information. Dialog Semiconductor furthermore takes no responsibility whatsoever for the content in this document if provided by any information source outside of Dialog Semiconductor.

Dialog Semiconductor reserves the right to change without notice the information published in this document, including without limitation the specification and the design of the related semiconductor products, software and applications.

Applications, software, and semiconductor products described in this document are for illustrative purposes only. Dialog Semiconductor makes no representation or warranty that such applications, software and semiconductor products will be suitable for the specified use without further testing or modification. Unless otherwise agreed in writing, such testing or modification is the sole responsibility of the customer and Dialog Semiconductor excludes all liability in this respect.

Customer notes that nothing in this document may be construed as a license for customer to use the Dialog Semiconductor products, software and applications referred to in this document. All use of Dialog Semiconductor products, software and applications referred to in this document are subject to Dialog Semiconductor’s Standard Terms and Conditions of Sale, available on the company website (www.dialog-semiconductor.com) unless otherwise stated.

Dialog and the Dialog logo are trademarks of Dialog Semiconductor plc or its subsidiaries. All other product or service names are the property of their respective owners.

© 2018 Dialog Semiconductor. All rights reserved.

Contacting Dialog Semiconductor

United Kingdom (Headquarters)
Dialog Semiconductor (UK) LTD
Phone: +44 1793 757700

Germany
Dialog Semiconductor GmbH
Phone: +49 7021 805-0

The Netherlands
Dialog Semiconductor B.V.
Phone: +31 73 640 8822

Email: enquiry@diasemi.com

Web site: www.dialog-semiconductor.com

North America
Dialog Semiconductor Inc.
Phone: +1 408 845 8500

Japan
Dialog Semiconductor K. K.
Phone: +81 3 5425 4567

Taiwan
Dialog Semiconductor Taiwan
Phone: +886 281 786 222

Singapore
Dialog Semiconductor Singapore
Phone: +65 64 8499 29

Hong Kong
Dialog Semiconductor Hong Kong
Phone: +852 3769 5200

Korea
Dialog Semiconductor Korea
Phone: +82 2 3469 8200

China (Shenzhen)
Dialog Semiconductor China
Phone: +86 755 2981 3669

China (Shanghai)
Dialog Semiconductor China
Phone: +86 21 5424 9058

10-Jan-2017