Abstract

The R-Car H3 System-on-Chip (SoC)-based platform from Renesas is part of a family of platforms (R-Car series) for automotive infotainment systems. The H3 is aimed at the high-end segment, and is optimized for automotive Human Machine Interface (HMI), infotainment and integrated dashboards.

The platform features the Dialog DA9063-A as system PMIC (Power Management IC) and the Dialog DA9213-A and DA9214-A multi-phase sub-PMIC step-down buck converters to power and supervise the complete system.

Through a description of the general system configuration, power capabilities and requirements and an overview of the component interconnections, it will be shown that the combination of DA9063-A, DA9213-A, and DA9214-A are highly suited as the R-Car power management system solution for H3 platforms.
DA9063-A Power Management for R-Car H3 Platform

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1 Introduction

This document describes how to interconnect the DA9063-A Power Management IC (PMIC) and the DA9213-A and DA9214-A sub-PMICs to the Renesas R-Car H3 System on a Chip (SoC). The DA9063-A is a highly integrated chip that supports Dynamic Voltage Control (DVC) technology, enabling significant power saving: this feature supports the Dynamic Voltage and Frequency Scaling (DVFS) technology that is used by many processors.

As a result of their highly integrated features, the DA9063-A PMIC, DA9213-A, and DA9214-A sub-PMICs significantly reduce the overall system cost and size compared to a discrete solution. This application note addresses only the power supply related features: discussion of other features of the optimized PMIC is beyond the scope of this document.

For further information on the DA9063-A, DA9213-A, and DA9214-A please refer to the datasheets available via your local Dialog sales office.

For information about Renesas R-Car H3 SoC, please refer to Renesas website:


2 Renesas R-Car H3 SoC Description

Renesas R-Car H3 is a platform for automotive infotainment with an SoC containing ten cores (ARM® Cortex®-A57 Quad Core, ARM Cortex-A53 Quad, ARM Cortex-R7 Dual lock-step) and PowerVR GX6650 GPU.

Figure 1 shows a typical system block diagram of the R-Car H3 SoC application. The embedded cores require suitable power management that is readily achieved using the Dialog DA9063-A, DA9213-A, and DA9214-A.
3 DA9063-A, DA9213-A, and DA9214-A Description

The DA9063-A (Figure 2) is a high-current system PMIC suitable for dual- and quad-core processors that require up to 5 A core processor supply. The DA9063-A contains:

- Six DC-DC buck converters designed to use small external 1 μH inductors, capable of supplying in total up to 12 A continuous output current (0.3 V to 3.3 V). The buck converters do not require external Schottky diodes; they dynamically optimize their efficiency depending on the load-current using an Automatic Sleep Mode (ASM) and incorporate pin and software controlled Dynamic Voltage Control (DVC) to support processor load adaptive adjustment of the supply voltage. In addition BuckPro includes the facility to implement VTT memory bus termination if required.

- 11 SmartMirror™ programmable low-dropout (LDO) regulators rated up to 300 mA. All support remote capacitor placement and can operate from low 1.5 V/1.8 V input supplies. This allows these LDOs to be cascaded with (in other words: supplied by) a suitable buck supply to improve overall system efficiency.

![Figure 2: DA9063-A System Block Diagram](image-url)
The DA9213-A (Figure 3) and DA9214-A (Figure 4) are multi-phase, single- and dual-output, synchronous step-down converters suitable for supplying CPUs that require high currents. Each converter operates using a small external 0.22 μH inductor on each phase. They produce an output voltage in the range of 0.3 V to 1.57 V. The input voltage range of 2.8 V to 5.5 V makes them suited to a wide variety of low-voltage systems.

To guarantee the highest accuracy and support multiple PCB routing scenarios without loss of performance, a remote sensing capability is implemented on each DA9213-A and DA9214-A output.

The DA9213-A buck operates with four phases and is capable of delivering up to 20 A continuous output current.

Each DA9214-A buck operates with two phases and is capable of delivering up to 10 A continuous output current per buck.
4 R-Car H3 SoC Power Requirements

Several power domains in the R-Car H3 SoC platform require precise voltage management for reliable system operation. The primary power domains are:

- DFVS_0.8V
- VDD_0.8V
- DDR_1.1V
- DDR_1.8V

Other supplies will be required for peripherals, I/O interfaces, SD cards, and such. Additionally, the system power management must comply with the specific power-up and power-down sequence guidelines for the R-Car SoC (shown in Figure 5).

Figure 5: Start-Up Sequence (Timing Is Not To Scale)

4.1 Memory Retention Mode

The R-Car H3 SoC implements a mode whereby the power supplies to the DDR memory are maintained during memory retention mode to preserve the memory contents. During memory retention the load current taken by the DDR memory is very low and all other supplies are disabled.

Figure 6 shows the PMIC interconnections for a system where all the DDR memory is powered as a single block. If the application necessitates splitting the memory architecture into two blocks this is shown in Figure 7. The second memory block can be enabled or disabled by the SoC enabling or disabling the rail switch controllers. In memory retention mode the second memory block will be powered down.
5 R-Car H3 SoC Power Tree System Diagram

Figure 6: R-Car H3 and PMIC Interconnections
6 R-Car H3 SoC Power Tree System Diagram (Split Memory)

Figure 7: R-Car H3 and PMIC Interconnections (Split Memory)
7  Cold boot Sequence for R-Car H3

Figure 8: DA9063-72-A Power-Up Sequence

Please contact your local Dialog representative for the recommended OTPs.
8 Operation

When 5 V is applied to the D5.0V and V_SYS supplies the DA9063-A system PMIC starts up automatically. It follows the start-up sequence programmed in the OTP enabling output power rails in the order specified. GPIO 7, 9, and 11 are configured to control the enabling of the three sub-PMIC bucks and are also part of the power sequencer timing. In this way the start-up timing of the sub-PMIC buck outputs are controlled.

Once the sequencer has completed the start-up sequence the nRESET signal from the DA9063-A is released to allow the SoC to start operation.

The outputs of LDO3 and LDO4 are combined to provide the specified 300 mA load current for the SD0 card supply. Similarly, LDO6 and LDO7 are combined as are LDO8 and LDO9 to power SD1 and SD2 cards respectively. LDO10 is a 300 mA LDO and can supply the SD3 card individually.

GPIO1, 2, and 13 provide the ability for the SoC to select the SD0-2 card output voltage by controlling the logic level applied to the GPIO input. A logic low from the SoC produces an SD card voltage of 1.8 V output on the respective output; a logic high produces an output of 3.3 V.

LDO5 is used to generate the internal power supplies for the Dialog system and sub-PMICs.

PMIC_RSTBn from the SoC is used to enter and exit memory retention mode. When PMIC_RSTBn is taken to a logic low the system PMIC performs a power-down sequence. During the power-down sequence the bucks supplying the DDR1.1V and DDR1.8V outputs are re-configured to prevent them from switching off.

Under normal ACTIVE mode conditions all bucks are programmed to operate in PWM mode to produce predictable noise performance. Efficiency is reduced at low load currents when operating in this mode so when entering memory retention mode the bucks supplying DDR1.1V and DDR1.8V are automatically changed to operate in Pulse Frequency Modulation (PFM) mode. In doing this the quiescent current from the 5 V input is reduced to less than 1 mA. If a split memory architecture is implemented then only Bank0 will be preserved during memory retention mode, Bank1 will be turned off.

When PMIC_RSTBn is taken to a logic high once more the DDR1.1V and DDR1.8V bucks are automatically re-configured to operate in Pulse-Width Modulation (PWM) mode before the system returns fully to ACTIVE mode by following the start-up sequence.
9 DA9063-72HK2-A Detailed Register Description

Key Settings
- Normal start-up
- Voltage monitor
- Buck Mem & Buck IO merged mode
- 2-wire control interface, standard speed
- RTC enabled
- LDO 3, 4, 7, 8, and 9 GPIO controlled by host for 1.8 V or 3.3 V SD card supply select

Table 1: DA9063-72HK2-A Register Settings

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<tr>
<th>Register Address</th>
<th>Function</th>
<th>Register Value</th>
<th>Register Description</th>
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<tr>
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<td>IRQ_MASK_A</td>
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<td>nONKEY, RTC, and some status IRQ masks</td>
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<td>IRQ_MASK_B</td>
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<td>Charger wakeup and temperature, current, or voltage IRQ masks</td>
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<td>GPI7 to 0 and ADCIN1-3 IRQ masks</td>
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<td>GPIO15 to 8 and external control signal IRQ masks</td>
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<td>CONTROL_A</td>
<td>0x03</td>
<td>PSM target status, companion charger control</td>
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<td>0x00F</td>
<td>CONTROL_B</td>
<td>0x09</td>
<td>Power-down / -up signalling</td>
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<td>0x010</td>
<td>CONTROL_C</td>
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<td>CONTROL_D</td>
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<td>Watchdog and LED blink control</td>
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<td>CONTROL_E</td>
<td>0x04</td>
<td>RTC, ecomode, feedback pins, V_LOCK</td>
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<td>0x013</td>
<td>CONTROL_F</td>
<td>0x00</td>
<td>Watchdog reset, shutdown, and wakeup</td>
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<td>Disable / pause blocks when below the PSS sequencer PD_DIS slot</td>
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<td>GPIO_MODE8_15</td>
<td>0x0E</td>
<td>GPIO8 to 15 mode control</td>
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<td>SWITCH_CONT</td>
<td>0xB0</td>
<td>Rail switches</td>
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<td>BCORE2_CONT</td>
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<td>BUCKCORE2 control</td>
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<td>BPRO_CONT</td>
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<td>BUCKIO control</td>
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<td>BUCKPERI control</td>
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<td>LDO1_CONT</td>
<td>0x00</td>
<td>LDO1 control</td>
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</tbody>
</table>
## Register Address	Function	Register Value	Register Description
0x027	LDO2_CONT	0x00	LDO2 control
0x028	LDO3_CONT	0x20	LDO3 control
0x029	LDO4_CONT	0x20	LDO4 control
0x02A	LDO5_CONT	0x80	LDO5 control
0x02B	LDO6_CONT	0x40	LDO6 control
0x02C	LDO7_CONT	0x40	LDO7 control
0x02D	LDO8_CONT	0x60	LDO8 control
0x02E	LDO9_CONT	0x60	LDO9 control
0x02F	LDO10_CONT	0x00	LDO10 control
0x030	LDO11_CONT	0x00	LDO11 control
0x031	SUPPLIES	0x00	Vibrator output level
0x032	DVC_1	0x00	Dynamic voltage control
0x033	DVC_2	0x00	Dynamic voltage control
0x034	ADC_MAN	0x20	ADC manual and automatic measurement control
0x035	ADC_CONT	0x01	ADC automatic measurement control
0x036	VSYS_MON	0xAA
0x083	ID_2_1	0x00	PSS sequence control
0x084	ID_4_3	0xAA	PSS sequence control
0x085	ID_6_5	0xA1	PSS sequence control
0x086	ID_8_7	0xAA	PSS sequence control
0x087	ID_10_9	0xAA	PSS sequence control
0x088	ID_12_11	0x08	PSS sequence control
0x089	ID_14_13	0x08	PSS sequence control
0x08A	ID_16_15	0x87	PSS sequence control
0x08B	ID_18_17	0x48	PSS sequence control
0x08C	ID_20_19	0x49	PSS sequence control
0x08D	ID_22_21	0x00	PSS sequence control
0x08E	ID_24_23	0x06	PSS sequence control
0x08F	ID_26_25	0x00	PSS sequence control
0x090	ID_28_27	0x05	PSS sequence control
0x091	ID_30_29	0x09	PSS sequence control
0x092	ID_32_31	0x10	PSS sequence control
0x095	SEQ_A	0xDC	PSS sequencer slot end points
0x096	SEQ_B	0x4F	PSS sequencer slot end points
0x097	WAIT	0x10	Power sequencer wait cycle
0x098	EN_32K	0xEA	RTC clocking control
0x099	RESET	0x48	Reset timer control
0x09A	BUCK_ILIM_A	0xFF	Buck current limit
0x09B	BUCK_ILIM_B	0xFF	Buck current limit
## Register Address | Function | Register Value | Register Description
--- | --- | --- | ---
0x09C | BUCK_ILIM_C | 0xF5 | Buck current limit
0x09D | BCORE2_CFG | 0x81 | BUCKCORE2 control
0x09E | BCORE1_CFG | 0x81 | BUCKCORE1 control
0x09F | BPRO_CFG | 0x81 | BUCKPRO control
0x0A0 | BIO_CFG | 0x81 | BUCKPRO control
0x0A1 | BMEM_CFG | 0x81 | BUCKMEM control
0x0A2 | BPERI_CFG | 0xA1 | BUCKPERI control
0x0A3 | VBCORE2_A | 0x6C | BUCKCORE2 voltage A
0x0A4 | VBCORE1_A | 0x5A | BUCKCORE1 voltage A
0x0A5 | VBPRO_A | 0x7F | BUCKPRO voltage A
0x0A6 | VBMEM_A | 0x7D | BUCKMEM voltage A
0x0A7 | VBIO_A | 0x7D | BUCKIO voltage A
0x0A8 | VPERI_A | 0x32 | BUCKPERI voltage A
0x0A9 | VLOD1_A | 0x3C | LDO1 voltage A
0x0AA | VLOD2_A | 0x3C | LDO2 voltage A
0x0AB | VLOD3_A | 0x78 | LDO3 voltage A
0x0AC | VLOD4_A | 0x78 | LDO4 voltage A
0x0AD | VLOD5_A | 0x14 | LDO5 voltage A
0x0AE | VLOD6_A | 0x32 | LDO6 voltage A
0x0AF | VLOD7_A | 0x32 | LDO7 voltage A
0x0B0 | VLOD8_A | 0x32 | LDO8 voltage A
0x0B1 | VLOD9_A | 0x32 | LDO9 voltage A
0x0B2 | VLOD10_A | 0x14 | LDO10 voltage A
0x0B3 | VLOD11_A | 0x22 | LDO11 voltage A
0x0B4 | VBCORE2_B | 0x3C | BUCKCORE2 voltage B
0x0B5 | VBCORE1_B | 0x5A | BUCKCORE1 voltage B
0x0B6 | VBPRO_B | 0x7F | BUCKPRO voltage B
0x0B7 | VPERI_B | 0x7D | BUCKPERI voltage B
0x0B8 | VBIO_B | 0x7D | BUCKIO voltage B
0x0B9 | VBMEM_B | 0x7D | BUCKMEM voltage B
0x0BA | VLOD1_B | 0x3C | LDO1 voltage B
0x0BB | VLOD2_B | 0x3C | LDO2 voltage B
0x0BC | VLOD3_B | 0x2D | LDO3 voltage B
0x0BD | VLOD4_B | 0x2D | LDO4 voltage B
0x0BE | VLOD5_B | 0x14 | LDO5 voltage B
0x0BF | VLOD6_B | 0x14 | LDO6 voltage B
0x0C0 | VLOD7_B | 0x14 | LDO7 voltage B
0x0C1 | VLOD8_B | 0x14 | LDO8 voltage B
0x0C2 | VLOD9_B | 0x14 | LDO9 voltage B
## Register Address | Function | Register Value | Register Description
---|---|---|---
0x0C3 | VLDO10_B | 0x32 | LDO10 voltage B
0x0C4 | VLDO11_B | 0x22 | LDO11 voltage B
0x0C5 | BBAT_CONT | 0x00 | Backup battery charger
0x0C6 | GPO11_LED | 0x00 | High power GPO PWM
0x0C7 | GPO14_LED | 0x00 | High power GPO PWM
0x0C8 | GPO15_LED | 0x00 | High power GPO PWM
0x0C9 | ADC_CFG | 0xE0 | ADC automatic measurement control
0x0CA | AUTO1_HIGH | 0x00 | ADC measurement thresholds
0x0CB | AUTO1_LOW | 0x00 | ADC measurement thresholds
0x0CC | AUTO2_HIGH | 0x00 | ADC measurement thresholds
0x0CD | AUTO2_LOW | 0x00 | ADC measurement thresholds
0x0CE | AUTO3_HIGH | 0x00 | ADC measurement thresholds
0x0CF | AUTO3_LOW | 0x00 | ADC measurement thresholds
0x105 | INTERFACE | 0xB9 | Host interfaces
0x106 | CONFIG_A | 0x86 | Host interfaces and other IOs
0x107 | CONFIG_B | 0x7F | VDD_FAULT comparator
0x108 | CONFIG_C | 0x50 | Buck duty cycle and clock polarity
0x109 | CONFIG_D | 0x01 | 
0x10A | CONFIG_E | 0xFF | BUCK and rail switch default settings
0x10B | CONFIG_F | 0x07 | LDO default and bypass mode settings
0x10C | CONFIG_G | 0xFF | LDO default settings
0x10D | CONFIG_H | 0xF0 | 
0x10E | CONFIG_I | 0x04 | 
0x10F | CONFIG_J | 0xE3 | 
0x110 | CONFIG_K | 0x80 | GPIO pull resistors
0x111 | CONFIG_L | 0x0A | GPIO pull resistors
0x112 | CONFIG_M | 0x00 | 
0x113 | CONFIG_N | 0x00 | 
0x114 | MON_REG_1 | 0x8A | 
0x115 | MON_REG_2 | 0xFC | 
0x116 | MON_REG_3 | 0x07 | 
0x117 | MON_REG_4 | 0xF4 | 
0x121 | GP_ID_0 | 0x01 | 
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0x125 | GP_ID_4 | 0x00 | 
0x126 | GP_ID_5 | 0x00 | 
0x127 | GP_ID_6 | 0x00 | 
### DA9063-A Power Management for R-Car H3 Platform

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<thead>
<tr>
<th>Register Address</th>
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Status Definitions

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<th>Definition</th>
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<td>The content of this document is under review and subject to formal approval, which may result in modifications or additions.</td>
</tr>
<tr>
<td>APPROVED or unmarked</td>
<td>The content of this document has been approved for publication.</td>
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