Abstract

The DA9052 battery charger offers fully automatic operation as it is able to work without any external intervention from the host processor. The charging parameters are set in OTP and can meet the requirements of most handheld applications. This paper provides insight into common application cases, thus helping the designer choose the right settings.
The DA9052 High Efficiency Autonomous Charger

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1 Terms and definitions

CV          Constant voltage
CC          Constant current
PHY         Physical layer
EOC         End of charge
RTC         Real time clock
EMI         Electro-magnetic interference
Tjunc       Junction temperature
C rate      A charge or discharge current specified as a fraction of the battery capacity
2 Introduction

With reference to Figure 1, the main building blocks of the charger are:

- External P-channel MOSFETs at VBUS and DCIN. These provide protection for the internal circuitry. VBUS_PROT and DCIN_PROT pins support charging at nominally 5 V, protected up to 5.6 V. The sensing inputs VBUS and DCIN can withstand voltages up to 12 V. Higher input voltages will damage the charger. Internal logic, acting on the gate pins VBUS_SEL and DCIN_SEL, enable and disable the external switches.

- Two internal switches manage the power routing into the VCENTER node – the real input of the charger buck.

- The charger buck transfers input power to VDDOUT with high efficiency. The output voltage is regulated to be VBAT + 200 mV with a minimum of 3.6 V, thus optimising the efficiency of the following linear stage.

- A linear charging stage with an active diode allows the current to flow through a low on-resistance path in both directions, between the main application rail VDDOUT and the battery rail VBAT.

- The internal rail VDDREF is supplied either from VCENTER or VDDOUT, depending on which is the higher voltage, ensuring the highest voltage of the system is always available for the internal core activities, RTC and so on.

![Figure 1: Charger block diagram](image-url)
3 External components

External components should be chosen by consideration of their parasitic characteristics (low DCR for the inductor, low MOSFET gate capacitance and $R_{DS-ON}$) and voltage and current ratings. Capacitors should be type X5R or X7R and coil saturation current at least 1.3 times greater than the maximum charger buck output current.

With reference to Figure 1 and Figure 2, the following components are the recommended external components for the charger to function correctly:

<p>| | | | |</p>
<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>M1</td>
<td>SOT-563-6 1.6 x 1.6 x 0.55 mm</td>
<td>ON Semiconductor NTZS3151P</td>
<td></td>
</tr>
<tr>
<td>M2</td>
<td>SOT-563-6 1.6 x 1.6 x 0.55 mm</td>
<td>ON Semiconductor NTZS3151P</td>
<td></td>
</tr>
<tr>
<td>M1 + M2</td>
<td>PowerPAK1212-8 3.3 x 3.3 x 1 mm</td>
<td>Vishay Siliconix Si7911DN</td>
<td></td>
</tr>
<tr>
<td>M3</td>
<td>SOT-23 3 x 2.6 x 1 mm</td>
<td>Vishay Siliconix Si2333DS</td>
<td></td>
</tr>
</tbody>
</table>

<p>| | | | |</p>
<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>L1</td>
<td>4.7 µH</td>
<td>3 x 3 x 1.2 mm</td>
<td>1.2 A ± 20 %</td>
</tr>
<tr>
<td>C1, C2</td>
<td>2.2 µF</td>
<td>0603</td>
<td>X5R ± 15 %</td>
</tr>
<tr>
<td>C3, C4</td>
<td>4.7 µF</td>
<td>0603</td>
<td>X5R ± 15 %</td>
</tr>
<tr>
<td>C7</td>
<td>10 µF</td>
<td>0805</td>
<td>X7R ± 15 %</td>
</tr>
<tr>
<td>C5</td>
<td>3 x 10 µF</td>
<td>0805</td>
<td>X7R ± 15 %</td>
</tr>
<tr>
<td>C6</td>
<td>2 x 1 µF</td>
<td>0402</td>
<td>X5R ± 15 %</td>
</tr>
<tr>
<td>C6</td>
<td>10 µF</td>
<td>0805</td>
<td>X7R ± 15 %</td>
</tr>
</tbody>
</table>

Figure 2: External components required for correct operation
4 Choosing the right charger parameters

The charging process of a Lithium-Ion battery can be divided into three phases:

- pre-charge
- constant current (CC) fast charge
- constant voltage (CV) or top-off charge

![Li-Ion battery charge profile](image)

**Figure 3: Li-Ion battery charge profile**

4.1 Pre-charge phase

If the battery voltage is lower than 2.9 V a pre-charge phase is started with a reduced current compared to ICHG_BAT (see Figure 3). The pre-charge current ICHG_PRE is selected in register R65<7:6>

Battery pre-charge mode is started and controlled automatically by DA9052. This is needed to ensure that a completely empty battery can be charged without the intervention of the host processor.

The pre-charge also handles the re-enabling of a battery pack where the internal safety switch has been opened (due to deep discharge). The safety switch is reset by applying a current through the diode into the safety switch, charging the battery cell up to about 2.8 V at which point the switch will close again. Using control BLINK_FIQ, DA9052 can drive a flashing LED connected to GPO10 or GPO11 that will indicate battery charging. The flashing will stop when the application is able to power up.

**ICHG_PRE selection**

The recommended ICHG_PRE value is less than 10 % of the nominal charging current in the fast-charge phase. The ICHG_PRE value can be set to be 20 mA, 40 mA or 60 mA in register R65<7:6> but should not be configured too low as this will cause the pre-charge phase to take longer than necessary.
4.2 Constant current (CC) fast-charge phase

If $2.9 \text{ V} < \text{VBAT} < \text{VCHG\_BAT}$, the DA9052’s charger performs fast-charging with constant current. This can be configured via the ICHG\_BAT parameter.

ICHG\_BAT selection

ICHG\_BAT, selectable on register R65<5:0>, affects the charge time and the battery life.

Charging with higher ICHG\_BAT:

- Increasing the charge current shortens the charge time. Although the end of the CC phase is reached more quickly with a higher charge current, the CV phase will take longer. Some chargers claim to fast-charge a Li-Ion battery in one hour or less. Such a charger eliminates the CV stage and goes directly to ‘ready’ once the voltage threshold is reached at the end of CC stage. The charge level at this point is about 70%. The topping charge typically takes twice as long as the initial charge.

- Moderate charging / discharging rates help to increase the number of cycles and thus the battery life. Lower charge current reduces the time in which the cell stays at its maximum voltage. (This is beneficial because prolonged high voltage promotes corrosion which shortens battery life).

For example, the charge current of a cobalt-based Li-Ion battery should not be higher than 0.5C although smaller batteries used for cell phones can be charged at 1C. Generally, when using a specific battery type, a balance should be found between the priority given to the battery life and the overall charging time.

![Figure 4: Cycle performance at various charge/discharge rates](image-url)
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4.3 Constant voltage (CV) phase

In this phase, a Li-Ion battery is close to its complete charge (also called ‘top-off charge’). When the battery voltage is close to VCHG_BAT, the constant voltage (CV) phase takes over. It is only in this phase that an End of Charge (EOC) condition can be detected and charging can be terminated.

The EOC condition is determined by the charge current threshold ICHG_END, specified by R89<7:0>. To prevent battery deterioration from continuous top-off charging, a new cycle will start only if the battery voltage drops below a configurable re-charge threshold specified by:

Recharge Threshold = VCHG_BAT – VCHG_DROP

VCHG_BAT selection

VCHG_BAT selects the target value for the battery voltage when fully charged. The value is selected in register R66<7:3> and can be set between 3.65 V and 4.425 V in 25 mV steps, which covers a wide range of Li-Ion battery options.

The suggested value for most common Li-Ion cells is 4.2 V (4.1 V for Li-Polymer). However the configuration of this parameter requires careful consultation of the battery’s datasheet as VCHG_BAT has a significant influence on the safety of the overall application.

Setting VCHG_BAT to a lower target voltage:
- Provides a longer battery life.
- Reduces the available capacity and thus the on-time for running applications.

Setting VCHG_BAT to higher target voltages:
- Increases the available capacity and thus the on-time for running applications.
- Setting VCHG_BAT too high causes over charging which is dangerous for overall safety, hence any overcharging must be avoided. Li-Ion batteries are designed to operate safely within their normal operating voltage but become unstable if charged to higher voltages. If a typical cell is charged above the normal operating voltage it causes plating of metallic lithium on the anode; the cathode material becomes an oxidizing agent, loses stability and releases oxygen. Overcharging causes the cell to heat up. If left unattended, the cell could burn, vent or explode.

VCHG_DROP selection

The VCHG_DROP parameter in register R67<6> is used to determine when the charging process of a discharging battery will be restarted following a successful End of Charge detection.

A discharged battery will be recharged if a battery charger is still connected and the system is supplied from the charger.

Low values of VCHG_DROP allow the battery to remain close to its maximum capacity, thus maximizing the run-time. This comes at a cost in terms of an increased number of charging cycles, which causes reduced battery life.

The suggested value for this parameter is 200 mV for reduced battery deterioration.
ICHG_END selection

The ICHG_END parameter in register R89<7:0> configures the current threshold that terminates a charging cycle. The charging current is measured automatically by the GP-ADC every 1 ms or 10 ms (depending on setting of ADC_MODE in register R82), and an average value is determined over the previous 10 seconds, thus filtering and smoothing peaks and sudden changes in current.

The ICHG_END parameter directly influences the duration of the charging phase and is typically set at a level of less than 10 % of the selected ICHG_BAT. Taking the example of an application with a battery capacity C = 1000 mAh, charged at 1C rate, the appropriate value for ICHG_END would be 100 mA or less. Different ICHG_END values have the following effect:

- A lower value causes a longer charging time but results in a more completely charged battery (see Figure 5).
- A too high value can produce a premature end of charge with reduced available battery capacity.

![Figure 5: Charge stages of a 4.2 V Li-Ion Battery](image)

To achieve a completely charged battery, charge time can be sacrificed by setting ICHG_END to be less than 10 % of ICHG_BAT. With reference to the previous example, C = 1000 mAh battery, a value of 50 mA is suggested instead of 100 mA.
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4.4 Connection and operation with DCIN / USB supplies

DA9052 implements a 3-way power path switch that automatically selects the power source for the system rail VDDOUT from either the wall charger DCIN, the USB connection VBUS or the Li-ion battery VBAT. Preference is given in the order DCIN then USB VBUS and finally VBAT.

The charging source devices are classified based on the current that they are able to provide:

Table 1: Charging input device types

<table>
<thead>
<tr>
<th>Source</th>
<th>Characteristic</th>
<th>Available Current</th>
</tr>
</thead>
<tbody>
<tr>
<td>USB</td>
<td>A USB hub or host: unconnected or suspended</td>
<td>Up to 2.5 mA</td>
</tr>
<tr>
<td>USB</td>
<td>A USB hub or host: connected and not suspended, not enumerated</td>
<td>Up to 100 mA</td>
</tr>
<tr>
<td>USB</td>
<td>A USB hub or host: connected and not suspended, enumerated</td>
<td>Up to 500 mA</td>
</tr>
<tr>
<td>USB</td>
<td>A USB host or hub charger: compliant with USB 2.0 specification</td>
<td>Up to 1.5 A</td>
</tr>
<tr>
<td>USB</td>
<td>A USB dedicated charger: compliant with USB 2.0 specification</td>
<td>Up to 1.3 A</td>
</tr>
<tr>
<td>DCIN</td>
<td>A wall charger with voltage and current characteristics defined by the vendor</td>
<td>Vendor specific</td>
</tr>
</tbody>
</table>

Figure 6: Connections of DA9052 battery charger
4.5 ISET_BUCK / ISET_DCIN / ISET_USB selection

ISET_BUCK can be set in register R62<3:0> and is the current limit for the charger buck stage in Figure 6. Its OTP value should always be set to 100 mA if USB charging is to be used as this is the initial limit allowed. If the system is battery less the value should be set to 1300 mA.

When a charger is detected, the value of this register is loaded from ISET_DCIN or ISET_USB. For USB, the detection of the charger can be performed by DA9052’s internal circuitry or by a USB transceiver (see Section 4.8 for details). Once charging is active, the limit may be changed by writing to ISET_BUCK via the control interface.

The charger buck has a very high efficiency. The use of a buck converter stage instead of a linear stage increases the overall charger efficiency and allows more (mean value) current to be supplied to the application than is drawn from the external supply.

![Typical efficiency of DA9052's charger buck](image)

**Figure 7: Typical efficiency of DA9052’s charger buck**

When connecting a wall charger or a USB charger to the charger inputs, it is sometimes suggested to force the external charger into current limit. By doing this, the supply voltage will drop and the portable device will not have to dissipate power caused by a large difference between supply and battery voltage.

This method is usually adopted by linear chargers, which have better efficiency when the drop-out voltage is the lowest possible. The DA9052 charger does not need to do this as the embedded DC-DC converter transforms the whole input energy into an appropriate combination of charging voltage and current. This may be useful for some external supplies though.
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4.6 VCHG_THR selection

External chargers also have power limitations. It is often the case that the external charger output voltage will drop significantly when a large amount of current is sourced. The reason for this could be due to the output impedance or a limitation of internal magnetic (or other) components.

The charger buck has a current limit, represented as a digital value in register R62<3:0>. If the current demands are bigger than those which the external charger can provide, the external charger output voltage will drop. The VCH_THR value represents the input voltage low limit for the DA9052 device, below which the ISET_BUCK value is reduced. This is designed to prevent the external charger voltage from completely collapsing. With the buck current limit reduced, the external charger output voltage can stay in its ‘safe zone’ and will still be able to supply the system and charge the battery at the same time.

By setting a low value of VCH_THR, even collapsing supplies can be used and compatibility with the new USB 3.0 charging standard can be achieved. (All hubs and peripheral devices are required to be operational down to 4 V with loads up to 900 mA current).

Care must be taken when setting low values. The lowest value of VCH_THR for any system must be greater than the highest output voltage programmed for any of the regulators.

<table>
<thead>
<tr>
<th>NOTE</th>
</tr>
</thead>
<tbody>
<tr>
<td>Current-limited chargers provide more power at higher output voltages. Configuring VCH_THR too low creates a risk that the external supply/charger disconnects due to overload.</td>
</tr>
</tbody>
</table>

The DA9052 charger has a charger attach comparator (CHG_ATT). The comparator detects if there is a voltage drop of 100 mV or more across VCENTER and VDDOUT (see Figure 1) and acts together with the charge detection comparators as an under voltage lock-out.
4.7 Dynamic charging current control

With reference to Figure 8, the following actions are performed if the charging source voltage collapses:

- Initially, the voltage at the charger input (DCIN or VBUS) falling below VCHG_THR forces the charger buck state machine to reduce the charger buck current limit step-by-step down to its minimum value.
- If the input voltage does not recover above VCHG_THR and the CHG_ATT comparator flags a voltage drop from VCENTER to VDDOUT of less than 100 mV, the charger buck is disabled as soon as the current limit reaches its minimum value. The output of the comparator can be read at any time by the host on register R2.
- If the input voltage recovers, the state machine starts to increase the current limit again until it reaches its programmed value.

![Figure 8: Profiles of charger current and voltage](image-url)
The application system load \( (I_{sys}) \) and the current for battery charging \( (I_{chg}) \) form a combined load on the charger buck output rail \( VDDOUT \). Depending on the current capability of the external charger source, charger buck current limit setting and system load level the following operating states will occur:

### Table 2: 3-way switch states

<table>
<thead>
<tr>
<th>State</th>
<th>Load condition</th>
<th>Battery state</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>( I_{sys} + I_{chg} &lt; I_{buck} )</td>
<td>Charging at up to ( I_{CHG_BAT} ) current</td>
</tr>
<tr>
<td>B</td>
<td>( I_{sys} + I_{chg} &gt; I_{buck} &gt; I_{sys} )</td>
<td>Charging at reduced current level</td>
</tr>
<tr>
<td>C</td>
<td>( I_{sys} &gt; I_{buck} )</td>
<td>Discharging</td>
</tr>
</tbody>
</table>

A. If the combined load does not exceed the input current limit \( ISET\_BUCK \), then the charger buck delivers the needed load current without restrictions. In addition, the \( VDDOUT \) voltage will be regulated to 200 mV higher than \( VBAT \) to minimize the power consumption of the linear charger stage (see Figure 9).
B. If the combined load exceeds the input current limit $I_{SET\_BUCK}$, the linear charger stage automatically reduces the battery charge current to keep supplying the required system power. This is realised by reducing $V_{DDOUT}$ down to $V_{BAT}$, which consequently reduces the charging current. It is then possible to charge the battery with any surplus current that is not required by the application (see Figure 10).

Figure 10: Current path from valid USB according to state B.
C. If the application load alone exceeds input current limit ISET_BUCK, the battery linear charger shuts off completely and the extra power is drawn from the battery via the active diode (see Figure 11).

D. If the battery is deep discharged, VDDOUT will drop down to 3.6 V. If the buck continues to stay in current limit, the charging current will be automatically regulated down (see Figure 12) until VDDOUT = 3.4 V. The Host can detect a charging current less than ICHG_THD (to be set on register R88) by reading the status bit CHG_LIM in register R2.
E. If the battery is deep discharged, the battery current is already reduced to zero and the load current at VDDOUT exceeds the current limit at the charger, VDDOUT will range down to a level between 3.6 V and the battery voltage, indicated by the yellow region in Figure 13.

![Figure 13: Charger buck - VDDOUT vs VBAT](image)

Figure 13: Charger buck - VDDOUT vs VBAT

Figure 14, shows a DA9052 charger measurement with a USB supply connected with ISET_BUCK = 500 mA. In the first phase, the battery is charged with ICHG_BAT = 300 mA. The system load increases on VDDOUT and the USB input is able to provide the needed current.

![Figure 14: Power path, charger and system load measurements.](image)
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NOTE
The DA9052 switching charger always provides more current to the system (I_{bat} + I_{load}) than drawn from VBUS (I_{usb}), which reduces power dissipation and increases efficiency. It allows faster charging and a higher system load from a current limited supply (for example, up to 700 mA from a USB 500 mA charger).

As shown in Figure 9, the linear charger MOSFET provides a controlled current flow into the battery for charging purposes. During discharge this same device acts an active diode to provide a low impedance current path from the battery to VDDOUT. This occurs automatically as soon as the VDDOUT voltage drops below VBAT. When the active diode is engaged, it has approximately 140 mΩ on resistance.

If a lower on resistance is required during discharge, an external MOSFET should be used to supplement the internal active diode. It must be connected on the board and activated in control register R15 (0x0F). The external MOSFET is turned off during charging.

A MOSFET such as the Vishay Si2333 is suited to the purpose. (Qualitative results are shown in Figure 15).

![Figure 15: On-resistance of internal and external active diode.](image-url)
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Figure 16: Current path from valid USB according to state C and external active diode

4.8 CHG_USB_ILIM setting and use of D+ / D-

For USB-supplied applications the charger of DA9052 is part of a more complex system, therefore mutual interactions must be considered and overlapping functionalities should be taken into account.

The basic building blocks of such a system are shown in Figure 17. They can be summarised as follows:

● The DA9052, providing power to the circuits. Apart from supplies and other functions, it includes a charger block and a USB charger detection function connected to D+/D- pins.
● The lithium-Ion battery.
● The host processor.
● The USB transceiver (or PHY): it can be a separate transceiver or integrated into the host processor.
● The USB connector (Data, VBUS, GND).
Control CHG_USB_ILIM in DA9052 register R62<6> can be set either to ‘Auto’ or ‘Not Auto’ which determines the method of USB detection. If the bit is asserted, the USB current capability of the attached USB device (host or charger) is determined by the DA9052 via a procedure described in the datasheet. The procedure is compliant with the USB Battery Charger Specification. If the bit is set low, the negotiation has to be done by the external USB PHY.

It is important to avoid having the DA9052 and the external USB transceiver attempt to control D+/D- simultaneously.

The following sections detail some typical scenarios. These illustrate why the DA9052 should be configured with CHG_USB_ILIM = 1 in the OTP settings (loaded during powering up from RESET mode and after waking up from POWERDOWN mode); and why the host should always set CHG_USB_ILIM = 0 as soon as the system is powered up. All USB activities, including further charger supply detections, will then be handled by the USB PHY.

### 4.8.1 Host active – good battery

In the case of a good battery and host in active mode the correct choice is to enable the USB PHY on D+/D- and disable any activity by the DA9052 on D+/D-.

R62 should be configured with CHG_USB_ILIM = 0.

When a USB device is attached to the USB connector, the host is active and the USB PHY enumerates the maximum charge current. This will also ensure connection (D+/D- assertion) within 100 ms.
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4.8.2 Host idle (power down) – good battery

There are two possible settings adopted when the host is in power down:

- Some applications allow the USB PHY to run in power down mode. Usually a voltage regulator remains active to supply 1.8 V USB low voltage. In this situation, it is recommended to not activate the DA9052’s D+/D- negotiation because of functional overlapping on driving both the D+/D- lines (CHG_USB_LIM = 0). In the case of a USB connector being inserted, the USB PHY can immediately manage the maximum charge current enumeration to control the charging phase.

If the overall system current consumption has higher priority, the USB PHY can be turned off when the host is in power down. As in the above case, setting CHG_USB_LIM = 0 is recommended. The DA9052 can generate a wake-up and start a power-up of the system (see Figure 18). To be compliant with USB 2.0 and the Battery Charging Specification requirement to connect within 100 ms of starting to pull 100 mA, the power-up sequence of the host has to be faster than 90 ms (100 ms – 10 ms debounce), but this should be achievable for most applications.

![Figure 18: Example of start-up from idle, USB-PHY off, with good battery](image)

If, for any reason, during the host’s idle time the battery becomes weak or dead, then DA9052 sets VDD_FAULT and moves to RESET mode. A fast power up sequence can no longer take place. The host is moved to the power off state and the only possibility for a restart is to connect an external supply or insert a charged battery.
4.8.3 Host power off – weak or dead battery

This is the situation covered by the ‘Dead Battery Provision’ in the USB Battery Charging Specification.

- A downstream device is able to draw a suspend current of up to 2.5 mA average before the device is connected.
- A device with a dead, weak or no battery is allowed to draw up to 100 mA for up to 100 ms after attaching, in order to determine if it is likely to be able to connect. After this time, if the device determines that it definitely will not be able to connect, then the device shall reduce its current draw to less than 2.5 mA average (Dead Battery – no connect specification).
- The device is allowed to draw up to 100 mA max for more than 100 ms after attaching provided it uses this current to power on and connect. This is the usual case for applications including a USB data interface (see Figure 17).

Depending on the type of application there are two possible scenarios:

a. The system can start up with maximum 100 mA, turn on the USB PHY, connect and after connecting continue drawing 100 mA until the charger supply detection is performed by the USB PHY. (see Figure 19)

b. Many portable devices require more than 100 mA to power up. In this case the only possibility to be compliant with the USB Battery Specification is to use the 100 mA for longer than 100 ms just for battery charging purposes. Upon reaching its weak battery threshold, the device is required to immediately power up and connect. The portable device is not allowed to delay connecting in order to go into modes that are unrelated to powering up and connecting (for example phone calls, playing games, songs, videos, WiFi connections and such like). (see Figure 20)

Figure 19: Allowed and disallowed power-up sequence from a weak or dead battery
The USB Battery Charging Specification recommends that the PMIC plays an active role in the charger supply detection. After a portable device detects VBUS, it is allowed to check if the attached device is a charger by applying a voltage to D+ and checking the voltage on D-.

When a USB device has been attached to VBUS and CHG_USB_ILIM = 1 (set in the OTP registers) DA9052:

1. exits Reset mode and reads the OTP setting after a 10 ms debounce
2. drives the D+/D- circuitry (assuming the extern USB PHY is off) to detect the device type attached to VBUS. For a dedicated charger, DA9052 must detect a maximum resistance of 200 Ω between D+ and D-.

A dedicated wall charger or USB host/hub charger can be differentiated from a USB host/hub and can usually provide charging currents greater than 100 mA.

According to the USB Battery Charging Specification, if a charger is detected by the D+/D- circuitry, a higher charging current can be drawn and the system can power up with this higher current.

The Dead Battery Provision methodology is sketched in Figure 21.
The operations required to allow a good power up in the presence of a weak or dead battery that complies with the USB Battery Charging Specification are:

- Set CHR_USB_ILIM = 1 in the OTP of DA9052 to allow charger supply detection by the PMIC.
- The host sets CHG_USB_ILIM = 0 in DA9052 before it enables the USB transceiver.
- The host enables the USB PHY as soon as it is powered up.
- The host can decide whether to keep the USB PHY on or off before going into Idle mode.

There is the possibility that the application cannot run with a dead or weak battery, for example if DA9052 D+/- detects a USB supply with a limited current capability, for example 100 mA (normal host or hub, not charger).

In this case the application will try to start, but since the supply cannot provide enough power the system voltage will collapse when the current is drawn and DA9052 will sequence back into RESET mode due to a VDD_FAULT detection. On reaching RESET mode, the application will automatically stop drawing current and the external supply will usually then recover. In particular, applications that automatically boot whenever an external supply is detected would then fall into an endless shutdown-reboot loop (supply lockout) and will not be able to power up from this supply. For this condition, DA9052 provides an additional ‘Emergency Charging’ mode (see appendix A.3). Any automatic system power up will then be temporarily disabled and only the battery is charged with the available current for the time needed to be sufficiently charged. After that the application can start normally. Until then, a blinking LED can be activated informing the user of this charging phase.

Figure 21: Detection timing with DA9052 D+/- from dead or weak battery
Figure 22: Detection flow-chart for DA9052’s D+/D- with weak or dead battery
5 PCB layout guidelines

Careful printed circuit board (PCB) design is crucial to ensure good application electrical performance when using DA9052’s charger. Although the DA9052 is principally an analog power management device, it also includes high-speed digital functions which require specific rules to be followed. This section provides PCB layout guidelines specific to the DA9052 charger.

5.1 Recommendations on power lines

- Use wide traces for power supply lines. It is important to check in advance the maximum current flowing in each power trace. Such traces must have a width properly dimensioned to the current. Where possible, it is useful to add large copper areas. This minimises parasitic voltage drops, line inductances and switching transients.
- If connections are needed to different layers, the number of via holes used for the connections must be properly dimensioned to the routed current. If the number is too low, the parasitic resistance is increased and the reliability of the PCB is compromised.
- Avoid loops in the supply distribution traces. Loops carrying high current behave as antennas. Electromagnetic radiation may corrupt the correct function of other circuits on the PCB or cause EMI test failures.

5.2 Recommendations on sensitive lines

The DA9052 charger makes use of some sensitive analog lines (for example VBUS or DCIN used for sensing the voltage at the input of the external connected charger device) and some high-speed digital connections (for example D+/D- lines). Other digital connections may be needed in the application and may be routed close to the charger lines. High-speed digital signals include fast transitions between logic levels that contain high-frequency components. These are easily coupled onto adjacent traces and circuits, potentially causing signal corruption.

- On the PCB, sensitive analog lines and digital signals should be routed at maximum distance from each other.
- These lines should be isolated via intermediate ground planes or should be isolated within the same plane.

![Figure 23: Routing of sensitive analog lines and digital traces](image_url)
5.3 Analysis of the DA9052 charger pin connections

Table 3: DA9052 charger pin connections

<table>
<thead>
<tr>
<th>PAD</th>
<th>LINE TYPE</th>
<th>PAD NAME</th>
<th>PAD DESCRIPTION</th>
</tr>
</thead>
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<tr>
<td>49</td>
<td>digital</td>
<td>VBUS_SEL</td>
<td>Control for external over voltage protection and input selection of VBUS</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>To be connected to gate of PFET</td>
</tr>
<tr>
<td>47</td>
<td>high current</td>
<td>VBUS_PROT</td>
<td>OV protected VBUS charger input</td>
</tr>
<tr>
<td>84</td>
<td>sensitive analog</td>
<td>VBUS</td>
<td>USB or wall charger input</td>
</tr>
<tr>
<td>50</td>
<td>digital</td>
<td>DCIN_SEL</td>
<td>Control for external over voltage protection and input selection of DCIN</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>To be connected to gate of PFET</td>
</tr>
<tr>
<td>48</td>
<td>high current</td>
<td>DCIN_PROT</td>
<td>OV protected DCIN charger input</td>
</tr>
<tr>
<td>85</td>
<td>sensitive analog</td>
<td>DCIN</td>
<td>Wall charger input</td>
</tr>
<tr>
<td>83</td>
<td>sensitive analog</td>
<td>VCENTER</td>
<td>Protected input for switching charger (decouple with 10 uF)</td>
</tr>
<tr>
<td>46</td>
<td>high current</td>
<td>VSW</td>
<td>Switching node for charger buck</td>
</tr>
<tr>
<td>45</td>
<td>high current</td>
<td>VDDOUT</td>
<td>System power supply output</td>
</tr>
<tr>
<td>43</td>
<td>digital</td>
<td>AD_CONT</td>
<td>Active diode controller output</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>To be connected to gate of PFET (leave unconnected, if not used)</td>
</tr>
<tr>
<td>44</td>
<td>high current</td>
<td>VBAT</td>
<td>Connection to main battery</td>
</tr>
<tr>
<td>41</td>
<td>high speed digital</td>
<td>D+</td>
<td>USB D+</td>
</tr>
<tr>
<td>42</td>
<td>high speed digital</td>
<td>D-</td>
<td>USB D-</td>
</tr>
</tbody>
</table>
Figure 24: Example of layout for DA9052's charger

With reference to Figure 24:

- DCIN_PROT, VBUS_PROT, VSW, VDDOUT and VBAT are high current lines and therefore have a larger track width and at least two via holes. It is very important to reduce the voltage drop across the lines, because any drop will be added to the battery charging path or to the application’s supply path. It is important that these pins are connected to larger copper planes to mitigate pass transistor heat dissipation issues.

- VDDOUT node includes at least 30 µF of bypass capacitance (see Figure 2). Ceramic capacitors are highly recommended. This capacitance should be split into multiple capacitors, but most should be located near the heaviest load in the application.

- VBUS and DCIN are analog lines used for sensing the voltage on these inputs. The tracks do not need to be wide but particular care should be taken with regards to crossing noisy or high speed digital lines (see Figure 23).

- VBUS_SEL, DCIN_SEL and AD_CONT are low speed digital signals for the activation of external components. No particular care needs to be taken when routing these lines.
VCENTER is the input of the charger buck. The connection to the VCENTER capacitor must be done with increased width and be as short as possible (see Figure 25). No vias should be used in this connection. This is in order to minimize the parasitic inductance and resistance on this path, which could otherwise cause malfunction of the buck current sensing.

Figure 25: Example of connection of VCENTER to the capacitor
5.4 Routing D+/D- USB lines

A key feature of the USB-compliant charging modes of DA9052 is the detection of a USB-charger. This is defined by the Battery Charging Specification revision 1.0 of the USB Implementers Forum, and by the People's Republic of China (PRC) Ministry of Industry and Information Technology (MIIT) 'Telecommunications Industry Standard of the PRC'.

The USB specification requires a compliant charger to have an output of 5 V ±10 %, with a minimum current of 500 mA. The D+ and D- lines shall be connected together with a resistance less than 200 Ω, and be floating with respect to other pins. The PRC specification is the same, except the minimum current is not specified.

Both of these specifications require the D+ and D- signal lines to be connected to the DA9052 PMIC in order for the device to detect the charger without software intervention. To do this without affecting the USB2.0 signal integrity while the bus is used in a communication mode requires some care.

Connections between the USB connector and the USB interface device (USB PHY) are normally kept short, routed with a 90 Ω differential impedance and great care is taken to avoid crossing other signal tracks and ground plane breaks. Stubs must be avoided in the signal path, and hence pull-up resistors and protection devices are connected directly to the signal path (see Intel specification 'High Speed USB Platform Design Guidelines Rev1.0').

Figure 26 shows the recommended routing for two pairs of USB D+/D- signals relative to each other and other signals.

Dimensions are in mils (0.025 mm). These vary slightly, depending on board, layer and copper thickness.

In order to respect these requirements, the connections to the D+ and D- terminals of DA9052 cannot be made to the route from the USB PHY to the connector.

The optimum connection is to route directly from DA9052 D+/D- to the USB PHY with 90 Ω differential impedance tracks. Isolation resistors should be included in the lines close to the PHY to allow isolation or modification of the trace impedance.
This will ensure that the communication channel is unaffected by the extra routing to the PMIC. It can be a challenge to make these connections at the USB PHY, but the suggested layout below shows a possible approach.

![Diagram of suggested layout for D+/D- lines]

**Figure 28: Suggested layout for D+/D- lines**
5.5 Alternative approaches

Routing from the USB PHY to the DA9052 represents a significant risk to communication integrity. There are two alternative approaches:

1. Use built-in multiplexer switches in the USB PHY.

Many USB PHY devices (such as USB3329 from SMSC Corp) include a multiplexer at the D+/D- pins. These are provided to allow other devices, primarily audio devices, to connect to the USB bus when normal communications are not used. The same multiplexed pins can be used by the charger detection circuitry on DA9052 without compromising data integrity.

2. Use external multiplexer.

Dedicated multiplexer devices are available (for example Fairchild FSA223) which can be inserted into the data path. The pin locations on such devices are such as to allow the 90 Ω differential path to pass through relatively undisturbed.

![Figure 29: Example of connection by means of multiplexer integrated in USB PHY](image1)

![Figure 30: Example of connection by means of external multiplexer](image2)
6 Frequently asked questions

6.1 When DA9052 is in POWERDOWN mode, is the charger active or not?

The battery charger of DA9052 can be configured to be switched on or off in POWERDOWN mode (see register R18<4>). If the bit is asserted, than the charger is switched off in POWERDOWN. If the bit is cleared, charging activities are also active in POWERDOWN.

- If an external USB or DCIN is already connected to the system, it is possible to leave the charger active also in POWERDOWN mode. Before powering down, the host processor needs to set the bit CHG_PD = 0. Then, even if the application is idle, the charging cycle can continue.

- For the lowest quiescent current when no USB or DCIN is connected to the system, it is recommended to disable the charger circuitry in POWERDOWN mode. The charger input will still be monitored and, when a supply is connected, it will be correctly detected and DA9052 will wake-up the application with an event (VBUS_DET or DCIN_DET).

6.2 What is the safety timer and how can it be used?

The battery charger of DA9052 provides a safety timer to limit the maximum battery charging time if normal end of charge conditions are inhibited (for example due to a broken battery pack). This is a safety feature to avoid uncontrolled charging. If battery charging does not terminate by means of current and voltage settings because the battery is faulty, this feature limits the total charging time and ensures termination after a duration that can be set in relation to the typical total battery charge time.

During fast charge mode, the time is dynamically extended whenever the current into the battery falls below ICHG_THD in register R88 (see Figure 12 and Figure 14 and Figure 32). This value should be programmed by the host to be 50 % of the configured maximum charge current ICHG_BAT. The change in charge time is inversely proportional to the change in charge current. The dynamic safety timer is limited to eight times the programmed time period. The default TCTR setting is 300 minutes.

If TCTR_MODE = 1 in register R67, the total charge time is fixed. With this configuration a continuous supervision of ICHG_AV is recommended to enable an appropriate handling of EOC from safety timer expiration. Alternatively the host processor may simply detect periods of reduced charge current by checking CHG_LIM in register R2. This status bit is asserted by DA9052 whenever the charging current drops below ICHG_THD.

Care must be taken when configuring the total charge timer TCTR (set in register R66 <3:0> and monitored in register R68). The host processor should initiate register R66 with the target value before starting charging, but should not overwrite (reset) the safety timer setting during a charging cycle.
6.3 How to monitor the temperature of the battery?

When the battery is being charged, the battery temperature is monitored automatically at the TBAT pin which is connected to the battery sense resistor (NTC behaviour) in the battery pack.

A 50 µA current source is driven through the battery temperature sense resistor, thus producing a voltage drop. This drop depends on the specific battery pack used and is always proportional to the temperature. A table of resistance versus temperature is needed in order to set the proper limits in DA9052 (See, for example, Figure 31 for the suggested 10 kΩ NCP15XH103J03RC).

The voltage at TBAT is read and converted by the ADC as part of the DA9052 scheduler in the auto ADC measurements. The result of the conversion is stored in register R90 TBAT_RES and can be read at any time by the host processor.

Recommended values for safe operation:

- R91 TBAT_HIGHP corresponding to 50 °C
- R92 TBAT_HIGN corresponding to 40 °C
- R93 TBAT_LOW corresponding to 0 °C

Example (ref Figure 31)

- R91: R is nearly 1/3 of the value at 25 °C, i.e. 3 kΩ and the voltage is 3 kΩ * 50 µA = 150 mV (corresponds to 0x0F).
- R92: R is nearly 1/4 of the value at 25 °C, i.e. 2 kΩ and the voltage is 2 kΩ * 50 µA = 100 mV (corresponds to 0x0A).
- R93: R is nearly 1.5 the value at 25 °C, i.e. 15 kΩ and the voltage is 15 kΩ * 50 µA = 750 mV (corresponds to 0x4C).

If three consecutive readings of TBAT are greater than TBAT_HIGHP or less than TBAT_LOW charging is disabled, an event flag is set and an interrupt E_TBAT is generated. The processor can then either service the IRQ and turn off charging or do nothing. If nothing is done, the FAST CHARGE block will start charging again as soon as the temperature readings are between the TBAT_HIGN and TBAT_LOW (for three consecutive readings). For minimum current consumption, it is suggested to set R82<5> TBAT_ISRC_EN = 0.
Figure 31: Resistance vs temperature for NCP15XH103J03RC
6.4 What happens if the Tjunc of the chip increases during charging?

During charging the junction temperature (Tjunc) of DA9052 is continuously supervised (thermal charge current control). A thermal supervision circuit automatically reduces the charge current via a current/temperature control if the die temperature rises above a preset value of 90 °C. It completely suspends charging if a temperature of 120 °C is reached.

The thermal charge current control can be disabled on register R62<7> CHG_TEMP = 0. This setting should be avoided.

![Figure 32: Thermal charge current control](image)

6.5 Is the DA9052 charger compliant to USB 2.0 in terms of inrush current?

The DA9052 charger is compliant with USB2.0 in terms of inrush current. The USB specification Rev 2.0 allows a maximum load equivalent to 10 µF capacitance to be placed at the downstream end of a USB cable in parallel with 44 Ω. These conditions ensure the correct voltage level on the bus. If more bypass capacitance is required, then the device must incorporate some form of VBUS surge current limiting, such that it matches the characteristics of the above load.

The DA9052 charger connects the USB input first to a 100 nF capacitor at VBUS_PROT and then (after charging it) to 2 x 4.7 µF capacitors at VCENTER. In both cases it is USB 2.0 compliant.

In the third phase, when the charging phase starts, the buck current is limited to 1.9 A for a maximum time of 20 us.

This leads to an equivalent capacitor of:

\[
C = \frac{1.9A \cdot 20\mu s}{5V} = 7.6\mu F
\]

- which is compliant to USB Rev 2.0.
6.6 Does DA9052’s charger support USB low power suspend mode?

The DA9052 charger supports USB low power suspend mode and is enabled via the control bit VBUS_SUSP in register R67. When enabled the VBUS_PROT path is switched off and the VDDOUT main supply is switched to the battery, disabling charging (similar to removing the VBUS supply).

VBUS_SUSP is cleared when the USB charger is removed. DCIN_PROT may also be temporarily disconnected via the DCIN_SUSP register bit. This function has a similar behaviour to VBUS_SUSP.

Additionally, DA9052 supports a USB bus-powered low current mode which is enabled via control bit CHG_BUCK_LP in register R62. In this mode the charger buck is forced to a PFM mode to ensure the system is backed up with minimum power dissipation when being supplied from an external supply. Charging will be suspended, but with appropriate configuration of the regulators, power to – for example an idle USB PHY – can be supplied.

<table>
<thead>
<tr>
<th>NOTE</th>
</tr>
</thead>
<tbody>
<tr>
<td>USB high power suspend mode allows max. 2.5 mA.</td>
</tr>
</tbody>
</table>
Appendix A

A.1 High voltage input protection

The external P-channel MOSFETs provide over-voltage protection up to 12 V. However the idle voltage of certain power supplies on the market can be as high as 28 V. The DA9052 is able to withstand such voltages by using the solutions described below.

A.1.1 Solution a

- Remove the external protection MOSFETs and short the DCIN and DCIN_PROT connections together.
- Incorporate an external over-voltage protection device set at 5.6 V (max). Charging is then allowed with an applied voltage of up to 5.6 V and the DA9053 is protected from higher voltages.

A.1.2 Solution b

Figure 33 shows a schematic using the internal logic of DA9052 to control an external over-voltage protection. It is shown for the DCIN input only, but can be implemented the same way on VBUS.

The protection MOSFET has been replaced by the high voltage capable circuitry in the yellow box (comprising two N-channel MOSFETs, one P-channel MOSFET, one zener diode with a zener voltage between 6 V and 12 V and three resistors). The DCIN voltage is always sensed on top of the zener diode. When 5.6 V is exceeded, DCIN_SEL in the DA9052 internal logic sets the gate of the NMOS high and thus disconnects the high side PMOS. R1 is used to limit the current through the Zener diode and R2 / R3 are passive pull-ups for the NMOS drains.

---

Figure 33: Proposed circuit for external over-voltage protection of the charger inputs up to 28V
A.2 Reverse polarity input protection

If the application charger input allows the connection of external supplies with reversed polarity, DA9052 can be damaged.

Figure 34 shows a circuit that provides protection against this scenario for the wall charger (the same applies for the USB input, if needed).

Under normal conditions (for example positive voltage 5 V at DCIN), the gate of the P-channel MOSFET is grounded through R1 and the device acts as a closed switch with low on-resistance. If a negative voltage is applied at DCIN (for example -5 V), the gate-source voltage is reversed and the switch is opened thus isolating the following circuitry.

The suggested P-channel MOSFET is the Fairchild Semiconductor FDZ191P in WL-CSP package and the resistor value should be 47 Ω. The Zener diode limits the maximum gate-source voltage applied to the MOSFET.

Figure 34: Proposed structure for external reverse polarity protection of the charger inputs
A.3 Emergency mode and LED blinking activation

Emergency mode allows any application to charge the battery from a low power charger even if the battery is deeply discharged.

If the host is not able to power up with the maximum available supply current, the application will initially try to start but, since the supply cannot provide enough power, the system voltage VDDOUT will collapse and the DA9052 will return to RESET mode after detecting a VDD_FAULT condition. After reaching RESET mode, the application will stop drawing current and the external supply will usually recover its output voltage. Applications that automatically boot up whenever an external supply is detected would then fall into an endless shutdown-reboot loop (supply lockout) and will not power up from this supply. However, DA9052 temporarily disables AUTOBOOT following the first shutdown to RESET mode and activates an Emergency (Charge) mode.

The supply can then charge the battery. When the battery voltage reaches (VDD_FAULT_UPPER) the battery is good and a wake up can be triggered by the user (GPIs or nONKEY).

During Emergency mode, an automatically-flashing LED can be enabled in order to inform the user that a charging process is in progress and that it is necessary for them to wait before being able to start the system. LEDs sinking up to 15 mA on either GPIO10 or GPIO11 can be used. These general purpose I/O ports must be properly configured in register R26 as open-drain outputs. Blinking in Emergency mode must be activated in OTP in register R16 <0:1>. Designed specifically as a visual indication to a user, the LED blinking is fixed at 0.5 Hz. A pulse duration of 10 ms or 40 ms can be selected.

Revision history

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<th>Description</th>
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<td>16-Apr-2009</td>
<td>Initial version.</td>
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<td>5.0</td>
<td>12-Feb-2016</td>
<td>Revise content and update to new corporate template</td>
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<tr>
<td>5.1</td>
<td>18-Feb-2016</td>
<td>Typographical corrections.</td>
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The DA9052 High Efficiency Autonomous Charger

Status definitions

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<td>The content of this document is under review and subject to formal approval, which may result in modifications or additions.</td>
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<tr>
<td>APPROVED or unmarked</td>
<td>The content of this document has been approved for publication.</td>
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