

User Manual

DA16200 SDK Memory Map

UM-WI-035

Abstract

This document describes the SRAM Memory Map of the DA16200 and how to manage the RW Data memory size.

DA16200 SDK Memory Map

Contents

Abstract 1

1 References 3

2 Introduction..... 3

3 SFLASH Memory Map..... 4

 3.1 2 MB SFLASH Memory Map..... 4

 3.2 4 MB SFLASH Memory Map..... 4

 3.3 Change SFLASH type..... 5

4 SRAM Memory Map..... 6

 4.1 Resize the Changeable SRAM Section 6

 4.2 Check the Changed SRAM Memory Size..... 8

Revision History 9

Figures

Figure 1: 2 MB SFLASH Memory Map 4

Figure 2: 4 MB SFLASH Memory Map 4

Figure 3: System Memory Map 6

DA16200 SDK Memory Map

1 References

- [1] DA16200, Datasheet, Dialog Semiconductor
- [2] DA16200, EVK User Manual, User Manual, Dialog Semiconductor
- [3] DA16200, SDK Programmer Guide

2 Introduction

The DA16200 SDK provides the 2 MB SFLASH for code and read- only data and the 512 KB SRAM for variable RW data and dynamic allocation.

This document describes how to change the map of SFLASH memory in the DA16200 SDK and to adjust the size of user RW-data and a heap memory area required for development of the products.

NOTE
The DA16200 SDK provides two types of SFLASH: <ul style="list-style-type: none">● ISSI IS25LP016D 2MB SFLASH● Winbond W25Q32JW 4MB SFLASH To change a SFLASH type, contact Dialog Semiconductor to confirm availability.

DA16200 SDK Memory Map
3 SFLASH Memory Map

The DA16200 SDK provides two types of a SFLASH memory map: 2 MB and 4 MB maps.

3.1 2 MB SFLASH Memory Map

The 2MB SFLASH memory map is a default map. If you compile without changing anything in the DA16200, the RTOS has the 2 MB SFLASH memory map.

0x0000_0000	2nd Bootloader	36 KB
0x0000_9000	Boot Index	4 KB
0x0000_A000	RTOS #0	924 KB
0x000F_1000	SLIB #0 (RamLib + TIM)	52 KB
0x000F_E000	RTOS #1	924 KB
0x001E_5000	SLIB #1 (RamLib + TIM)	52 KB
0x001F_2000	User Area	12 KB
0x001F_5000	Debug/RMA Certificate	4 KB
0x001F_6000	TLS Certificate Key #0	16 KB
0x001F_A000	TLS Certificate Key #1	16 KB
0x001F_E000	NVRAM #0	4 KB
0x001F_F000	NVRAM #1	4 KB

Figure 1: 2 MB SFLASH Memory Map

3.2 4 MB SFLASH Memory Map

The DA16200 SDK also supports the 4 MB SFLASH memory map.

0x0000_0000	2nd Bootloader	36 KB
0x0000_9000	Boot Index	4 KB
0x0000_A000	RTOS #0	1900 KB
0x001D_B000	SLIB #0 (RamLib + TIM)	64 KB
0x001F_5000	Debug/RMA Certificate	4 KB
0x001F_6000	TLS Certificate Key #0	16 KB
0x001F_A000	TLS Certificate Key #1	16 KB
0x001F_E000	NVRAM #0	4 KB
0x001F_F000	NVRAM #1	4 KB
0x0020_0000	RTOS #1	1900 KB
0x003D_B000	SLIB #1 (RamLib + TIM)	64 KB
0x0039_0000	User Area	84 KB

Figure 2: 4 MB SFLASH Memory Map

DA16200 SDK Memory Map

3.3 Change SFLASH Type

The DA16200 SDK supports 2 MB SFLASH memory map. To create an image for a 4 MB SFLASH memory map using the DA16200 SDK, change some files for 4 MB memory map as follows, and then execute the SDK Compile. See [3].

- 2nd Bootloader file : ~/SDK/build/SBOOT/image/ DA16xxx_ueboot.bin.4MB
➔ ~/ SDK/build/SBOOT/image/ DA16xxx_ueboot.bin
- Config file : ~/SDK/build/SBOOT/cmconfig/fc9ktpmconfig.cfg.W25Q32JW(4MB)
➔ ~/SDK/build/SBOOT/cmconfig/fc9ktpmconfig.cfg
- Load script file : ~/SDK/build/ldscripts/DA16xxx_rtos_cache.icf.4MB
➔ ~/SDK/build/ldscripts/DA16xxx_rtos_cache.icf
- Macro file : ~/SDK/build/macro/da16200_asic_cache.mac.4MB
➔ ~/SDK/build/macro/da16200_asic_cache.mac
- Compile feature : ~/SDK/src/customer/config_generic_sdk.h
#undef __FOR_4MB_SFLASH__ ➔ #define __FOR_4MB_SFLASH__

DA16200 SDK Memory Map

4 SRAM Memory Map

The DA16200 SoC has a total of 512 KB of SRAM. The overall memory map is organized as shown in Figure 3.

User can change and use the rest of the space except for the area used by the system. If you need more RW Data space, you can change the size of this area and reduce other spaces along with it.

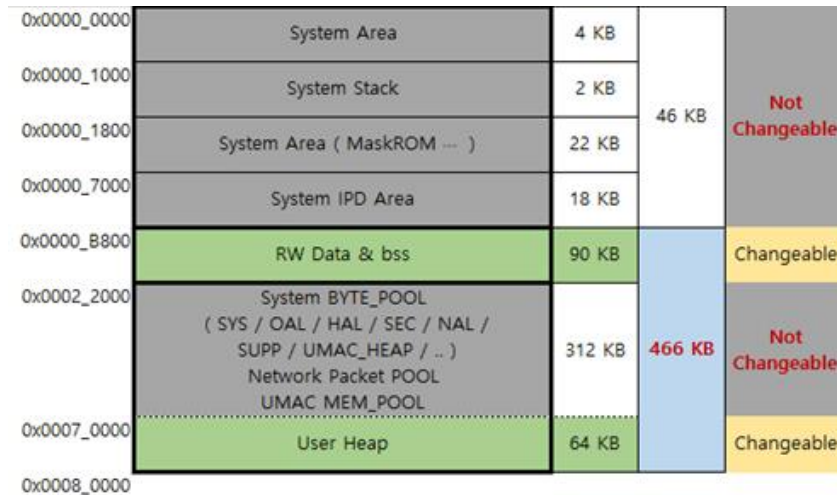


Figure 3: System Memory Map

4.1 Resize the Changeable SRAM Section

If you use the DA16200 SDK, to change the size of the memory area provided by default, do the following:

- Open the needed memory map configuration file located at ~/SDK/build/ldscripts. This folder has three configuration files:
 - DA16xxx_rtos_cache.icf for default 2 MB SFLASH
 - DA16xxx_rtos_cache.icf.2MB for 2 MB SFLASH configuration
 - DA16xxx_rtos_cache.icf.4MB for 4 MB SFLASH configuration

NOTE

These ICF files have different definitions of SFLASH size, but the memory map of the SRAM area is the same.

- Resize the changeable area marked green in Figure 3. The changeable areas are two parts of the SRAM memory map:
 - RW Data & .bss
 - User Heap

```

/*****
 * RAM regions
 *****/
define symbol __ICFEDIT_region_SYSRAM0_start__ = __ICFEDIT_sram_base__ +
0x00000000;
define symbol __ICFEDIT_region_SYSRAM0_end__ = __ICFEDIT_sram_base__ +
0x000003FF;
define symbol __ICFEDIT_region_SYSRAM1_start__ = __ICFEDIT_sram_base__ +
0x00000400;
define symbol __ICFEDIT_region_SYSRAM1_end__ = __ICFEDIT_sram_base__ +
0x000005FF;

/* System STACK : 2 KB : Total 6 KB */

```

DA16200 SDK Memory Map

```

define symbol __ICFEDIT_region_STACK_start__ = __ICFEDIT_sram_base__ +
0x00001000;
define symbol __ICFEDIT_region_STACK_end__   = __ICFEDIT_sram_base__ +
0x000017FF;

/* System IPD : 18 KB                               : Total 46 KB */
define symbol __ICFEDIT_region_RAMIPD_start__ = __ICFEDIT_sram_base__ +
0x00007000;
define symbol __ICFEDIT_region_RAMIPD_end__   = __ICFEDIT_sram_base__ +
0x0000B7FF;

/* RAM : RW data area for RTOS : 90 KB               : Total 136 KB */
define symbol __ICFEDIT_region_RAM_start__    = __ICFEDIT_region_RAMIPD_end__ +
1;
define symbol __ICFEDIT_region_RAM_end__      = __ICFEDIT_sram_base__ +
0x00021FFF;

/* RAM : Heap & Pool Region : 376 KB (include Heap) : Total 512 KB */
/* Include
* System Byte Pool           : 195.5 KB
* Network Stack Packet Pool  : 46.0 KB ( 45.875 KB )
* UMAC Socket Buffer          : 72.5 KB
* Heap memory                 : 64.0 KB
*/
define symbol __ICFEDIT_region_FREE_start__ = __ICFEDIT_region_RAM_end__ + 1;
define symbol __ICFEDIT_region_FREE_end__  = __ICFEDIT_sram_base__ +
__ICFEDIT_sram_size__ - 1 ;

/* Generic Heap size : 64 KB */
define symbol __ICFEDIT_size_heap__        = 0x00010000;

```

NOTE

The size of the two changeable areas and the total size of the area used by the system cannot exceed 512 KB.

The total memory sections are defined as below:

```

place in ROM_region {
    first section .text
    , section .rodata
    , readonly
};

place in RAM_region {
    first section RW_SEC_HAL
    , section RW_SEC_KERNEL
    , section RW_SEC_LIB
    , section RW_SEC_OAL
    , section RW_SEC_UNINIT
    , section RW_SEC_ZERO
    , section RW_SEC_CLK
    , section RW_SEC_DMA2ND
    , section .bss
    , readwrite
};

place in SYSRAM0_region {

```

DA16200 SDK Memory Map

```

        section RW_SEC_DMA
        };

place in SYSRAM1_region {
        section RW_SEC_NVIC
        };

place in STACK_region {
        block CSTACK
        };

place in RAM_freemem {
        first section FREE_MEM
        , last block HEAP
        };

place in RAMIPD_region {
        first block RAMIPD
        };

```

4.2 Check the Changed SRAM Memory Size

After the compile is done for the default values or the changed values, you can check the file compiled result as following:

1. Open the compiled memory map file.

~/SDK/build/asic/Release/List/main_libndk_cache.map

This file includes the description of each memory section.

"A1": place at 0x00101400 { ro section .intvec, ro section .asmtext };

"P1": place in [from 0x00101400 to 0x001e6fff] {
first section .text, section .rodata, ro };

"P2": **place in [from 0x0008b800 to 0x000a1fff]** {
first section RW_SEC_HAL, section RW_SEC_KERNEL, section RW_SEC_LIB,
section RW_SEC_OAL, section RW_SEC_UNINIT, section RW_SEC_ZERO,
section RW_SEC_CLK, section RW_SEC_DMA2ND, section .bss, rw };

"P3": place in [from 0x00080000 to 0x000803ff] { section RW_SEC_DMA };

"P5": place in [from 0x00081000 to 0x000817ff] { block CSTACK };

"P6": place in [from 0x000a2000 to 0x000fffff] {
first section FREE_MEM, last block HEAP };

"P7": place in [from 0x00087000 to 0x0008b7ff] { first block RAMIPD };

2. See the **P2** section that compiled the RW data & bss size part.

In this case, P2 size 0xe084 (57,476 B) is the final compiled RW data size.

```

"P2":
P2 mid-1          0x0008b800  0x1ef8  <Init block>
.data            inited  0x0008b800  0x50   system_start.o [1]

```

3. See the **P6** section to check the Heap memory size.

In this case, HEAP size 0x1000 (64 KB) is the final compiled Heap memory size.

```

"P6":
HEAP              0x000a2000  0x10000  <Block>
HEAP              uninit  0x000a2000  0x10000  <Block tail>
FREE_MEM          uninit  0x000b2000  0x10     tx_initialize_low_level.o [1]

```


Revision History

Revision	Date	Description
1.0	27-Nov-2020	Initial version.

DA16200 SDK Memory Map

Status Definitions

Status	Definition
DRAFT	The content of this document is under review and subject to formal approval, which may result in modifications or additions.
APPROVED or unmarked	The content of this document has been approved for publication.

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