Application Note

DA7212 Automatic Level Control Offset Calibration

AN-AU-024

Abstract

This document explains the DA7212 Automatic Level Control (ALC) system.

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1 Introduction

DA7212 contains a state of the art mixed signal Automatic Level Control (ALC) system. The ALC monitors the digital signal after the ADC and adjusts the microphone amplifier and digital ALC amplifier gains to maintain a constant recording level, whatever the analogue input signal level. The digital ALC amplifier gain is used for small gain steps and fast response whilst the microphone amplifier gain is utilised for large gain steps to preserve SNR. A second analogue amplifier in the mixer is also available for adding fixed analogue gain as shown in Figure 1.

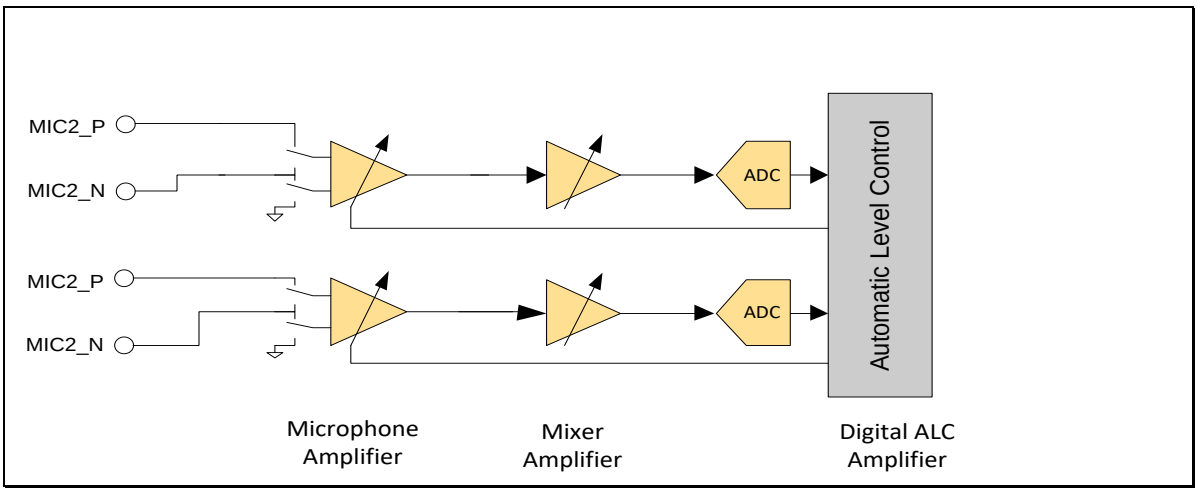

Figure 1: DA7212 ALC Architecture

The digital gain is updated in steps of 0.008 dB up to a maximum of 90 dB. The analogue gain is updated on a zero cross in steps of 6 dB up to a maximum of 36 dB as shown in Figure 2. To avoid pops, it is important that any DC offset between the analogue and digital amplifiers is eliminated. DA7212 provides an automatic calibration routine to cancel this DC offset and ensure pop and click free operation. The steps for performing this calibration are outlined in this document.

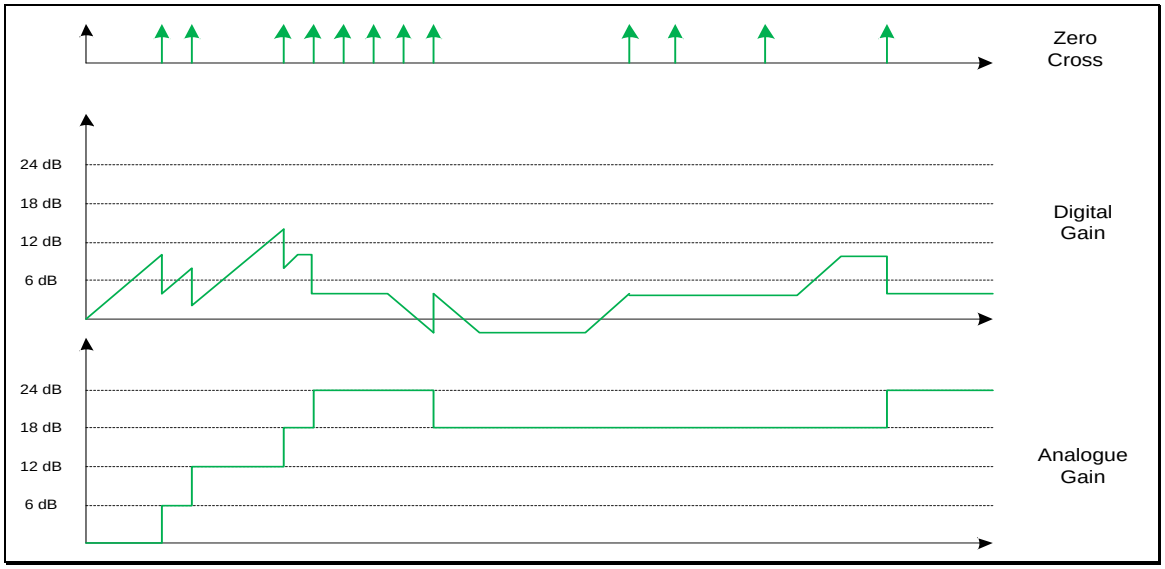

Figure 2: Digital and Analogue Gain Synchronization

2 When to Perform Offset Calibration

In a typical usage scenario offset calibration need only be performed when the device is enabled. However, to guarantee optimum ALC performance, the calibration should be performed whenever there is a major change in the recording path. Some examples of this are outlined in Section 3 including:

- When the record path is first instantiated
- When moving between different microphone sources. For example, when moving from an inbuilt microphone connected to MIC1_P and MIC2_P to an external microphone connected to MIC1_N and MIC2_N
- When altering the input mixer gain

3 Calibration Routine

The calibration routine requires the full signal path from microphone to ADC to be enabled and a clock to be present. The calibration routine using MIC1_P and MIC2_P and with the device in slave mode is outlined in .

Table 1: Offset Calibration, MIC1_P and MIC2_P Single-Ended, Slave Mode

Instruction	Registers Affected	Value
Enable Master Bias	0x23	0x80
Enable AIF and setup clocks (for 44.1 kHz, I2S, slave mode)	0x29	0xC8
Enable the Microphones unmuted	0x63 0x64	0x84 0x84
Mute the microphones	0x63 0x64	0xC4 0xC4
Enable the Input mixers unmuted	0x65 0x66	0xA8 0xA8
Route the microphone to the mixers	0x32 0x33	0x04 0x04
Enable the ADC unmuted	0x67 0x68	0xA0 0xA0
Calibrate Offset	0x2B	0x10
Wait until offset bit has been cleared	Wait until 0x2B=0x00	
Enable ALC	0x2B	0x8B
Unmute Microphones	0x63 0x64	0xA8 0xA8

Note 1 Other clocking and microphone setups are also possible by changing their respective registers. Once this calibration is complete, the record path with Automatic Level Control is active.

4 Troubleshooting

Take note that 0x2B should automatically clear after 256 samples (5.33 ms at 48 kHz). If 0x2B does not return 0x00 after 256 samples, this indicates a setup error. If this occurs, check that the microphone is enabled and muted, the mixer is enabled with the microphone input selected and unmuted, and that the ADC is enabled and unmuted. It is also critical that an MCLK and BCLK are present on the device. BCLK can be provided either from the AIF interface in slave mode or generated internally by having the device in master mode.

Revision History

Revision	Date	Description
1.0	15-Dec-2020	First Release

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Status Definitions

Status	Definition
DRAFT	The content of this document is under review and subject to formal approval, which may result in modifications or additions.
APPROVED or unmarked	The content of this document has been approved for publication.

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